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Defect-Mediated Carrier Transport Mechanisms in Vertical GaN *p-n* Diodes

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials

by

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December 2019

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2. Les Eastman Conference 2018, Speaker, *Dislocation Assisted Carrier Transport Mechanism in GaN Bipolar Devices Leakage*
3. 2019 International Conference on Nitride Semiconductors, Speaker, *Dislocation Assisted Carrier Transport Mechanisms in Forward Bias GaN p-n Junction Leakage*
4. **C. Robertson** et al., "Charged Dislocation Band Distortion: An Explanation for Observed Forward Bias Leakage Currents in GaN p-n Diodes", *JAP*
5. (In Internal Review) **C. Robertson** et al., "Modeling Dislocation-Related Reverse Bias Leakage in GaN p-n Diodes"
6. (In Internal Review) **C. Robertson** et al. "Threading Dislocation Dependence on Transport Properties in p-n Junctions Grown by NH3 Molecular Beam Epitaxy

ABSTRACT

Defect-Mediated Carrier Transport Mechanisms in Vertical GaN *p-n* Diodes

by

Christian Andrew Robertson Bayless

In recent years, GaN power semiconductor devices have been the focus of research and development due to the favorable material properties of the III-N system. III-N semiconductors have been widely used in high-speed transistors, visible and ultraviolet (UV) optoelectronics, and vertical power electronics. One of the major challenges to the performance of GaN power devices has been the ubiquitous presence of defects – mainly threading dislocations – in its substrates and epitaxial layers. Recent work has also revealed that Ca point defects are present in significant concentration in MBE-grown GaN around the world likely originating from ambient contamination or chemical-mechanical polishing (CMP) surface treatments and that these point defects are likely compensating n- and p-type GaN; furthermore, a systematic way of controlling these defects was also discovered.

The effect of Ca point defects on *p-n* junction diode behavior was studied by comparing the transport behaviors in samples with and without high Ca incorporation. It was determined that Ca does not have a substantial effect on the ideality factor of the diode. However, it was found that Ca has a significant effect on other aspects of the device demonstrated by an increase in p-GaN resistivity (+107%) and decrease in p-GaN contact resistivity (-35%) when Ca was present. A similar study was also performed to observe the effects of threading dislocation density on the transport properties of vertical GaN p-n junctions. As has been reported by other growth techniques, vertical GaN *p-n* diodes grown by NH_3-MBE

demonstrated substantial effects of threading dislocation density on leakage currents. These results were then compared to a simulation modeling leakage mechanisms of threading dislocations in vertical GaN *p-n* interfaces.

To study threading dislocations in GaN *p-n* junctions, advanced finite element analyses softwares were used to compare vertical GaN *p-n* diodes with and without a dislocation. At zero bias, it was observed that the depletion region width (using the Depletion Approximation) and the maximum electric field were reduced drastically near the dislocation line. More significantly, an asymmetric reduction in the diffusion barrier for electrons and holes was observed due to the asymmetric nature of the dislocation induced band bending related to the doping and trap parameters. The reductions in electric and diffusion barrier properties persisted into forward bias and asymmetric current profiles for electrons and holes were observed. Lastly, this diffusion barrier reduction carrier resulted in an additional leakage mechanism via Shockley-Read-Hall non-radiative recombination mediated by a high np-product and trap state density near the intersection of the dislocation with the junction.

This model was also used to simulate the dislocation mediated mechanisms in reverse bias on an identically structured diode with broader physical boundary conditions to account for depletion broadening. It was found that the defects coalesced by the dislocation strain field will mediate electron-hole pair generation by a trap-assisted tunneling mechanism occurring at a peak electric field in the junction near the dislocation. These electron-hole pairs are then swept away from the junction by the strong, reverse bias electric field thereby resulting in a reverse bias leakage current mediated by the dislocation trap states.

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Chapter 1. Introduction

Research Context

Before presenting the body of this research, it is first essential to understand some background on power conversion and electronics. Electrical power has become a fundamental part of modern society, but power does not typically exist in a form that is necessary at the point of application. Alternating current (AC) power is used to transport electricity long distances at high voltages (e.g., 300 – 500 kV) from the point of generation to the point of use, but most things used daily don't run directly on this 120 V_{rms} AC power. This requires that the AC power be converted into direct current (DC) power for many applications. Additionally, some applications such as electric vehicles store their energy in batteries that provide DC power, but this DC must be converted into AC to run electric motors efficiently. There are numerous other applications in which power must be converted, but AC-to-DC, DC-to-AC, DC-to-DC, and AC-to-AC conversions are essential to the modern world. These conversions all require circuitry and devices that can handle the loads imposed upon them without failing.

The devices within these power conversion circuits must be made of certain materials, thus it is important to understand what material properties are useful when considering different material systems for this set of applications. Although there are many such parameters, low intrinsic carrier concentration, high breakdown electric field, high thermal conductivity, and high saturation current velocity are the most broadly used for identifying and comparing power materials. A low intrinsic carrier concentration reduces the intrinsic conductivity of the material – this property is very important for ensuring that devices do not have a high reverse bias leakage current. A high breakdown electric field ensures that the devices made of the material under study have high fundamental limits to the voltages they can sustain without

failing; although other issues such as processes and defects play a role in breakdown events, ensuring that the device materials do not inherently fail at low voltage is essential for good power electronics. A high thermal conductivity aids a material's power electronic capabilities by allowing regions that may get hot during operation to transport that heat into appropriate heat sinking structures to prevent thermally induced damage to critical components. Lastly, a high saturation current velocity increases the limit of carrier transport velocity through the material thereby representing the maximum allowed current density that a material system can maintain. Materials that possess some or all these qualities are viable candidates for consideration in electronics for high power applications.

GaN for Power Electronics

In recent years, GaN power semiconductor devices have been the focus of research and development due to the favorable material properties of the GaN material system and its alloys. III-N semiconductors have been widely used in high-speed transistors[1–5], visible and ultraviolet (UV) optoelectronics[6–12], and vertical power electronics[13–17]. The high theoretical breakdown field (~3.3 MV/cm) and carrier mobility (>1,000 cm^2/V-s) have garnered interest in the field of power electronics where energy efficiency and high voltage operation are necessary.

A useful way of comparing material systems for specific applications is through comparative figures of merit (FoM). For power electronics, two useful FoMs were derived by Johnson[18] and Baliga[19]. The Johnson FoM characterizes the trade-off between maximum operating frequency and power amplification of transistors by using the product of the maximum voltage and frequency to create the following formulation

$$JF = V_{max} \times f_{max} = \frac{E_C v_{sat}}{2\pi}, \quad (1)$$

where E_C is the critical breakdown field of the material, and v_{sat} is the saturation current velocity. The Baliga FoM, in contrast, measures the trade-off between on-state resistance (ONR) and device breakdown. The formulation for the Baliga FoM is

$$BF = R_{on}^{-1} \propto \mu E_g^3, \quad (2)$$

where μ is the carrier mobility and E_g is the material band gap energy. Using these FoM as well as the raw material properties, different material systems can be evaluated for high power applications. The material properties of Si, 4H-SiC, and GaN are given in **Table 1** to contrast the theoretical limits of the materials systems that are current dominating this market and research environment.

	Si	**4H-SiC**	**GaN**	**Ga_2O_3**
E_g (eV)	1.1	3.26	3.4	4.8
n_i (cm^{-3})	1.5×10^{10}	8.2×10^{-9}	1.9×10^{-9}	5×10^{-22}
E_c (MV/cm)	0.3	2.0	3.3	8
V_{sat} (10^7 cm/s)	1.0	2.0	2.5	1.9
σ_{th} (W/m-K)	130	700	210	11
JFoM *	1	180	760	2844
BFoM *	1	130	650	3444

Table 1: Basic properties of major power electronics materials[20–22]. *The Johnson and Baliga Figures of Merit (FoM) are normalized to Silicon.

Based on the theoretical property limits of the materials, GaN appears to be the ideal choice for power electronics; however, GaN has several key research and industrial problems that must be addressed before it can become a dominant material in the market. Defect control in GaN growth has posed a substantial barrier to technological development. Until recently, homoepitaxial GaN growth was not viable as there was not a method of growing low defect GaN bulk crystals at a reasonable cost, thus industry and academia focused their efforts on

heteroepitaxial growth and its associated defects. Sapphire (Al_2O_3) became the preferred substrate due to its similar crystal structure, lattice parameter, and thermal expansion coefficients (shown in Table 2), but growth on sapphire always results in threading dislocation (TD) formation due to the chemical dissimilarity and lattice mismatch. Techniques were developed to grow decent quality GaN (threading dislocation density (TDD)$\sim 10^8$ cm^{-2}) on sapphire using metalorganic chemical vapor deposition (MOCVD), and these template growths can be used as homoepitaxial substrates in other growth techniques such as molecular beam epitaxy (MBE).

	Latt. Param. (Å)	**c-GaN Mismatch**	**α_v (10^{-6} K^{-1})**	**TDD (cm^{-2})**	**Cost**
GaN	a = 3.2 c = 5.2	0.0%	a = 5.6 c = 3.2	$10^4 - 10^6$	$$$$
4H-SiC	a = 3.1 c = 10.1	3.2%	a = 4.0 c = 4.0	$10^0 - 10^1$	$$
Al_2O_3	a = 4.8 c = 13.0	33%	a = 6.7 c = 5.0	$10^7 - 10^8$	$
Si	a = 5.4	41%	a = 2.6	10^{-1}	--

Table 2: Comparison of different growth substrates for GaN

GaN Crystallography

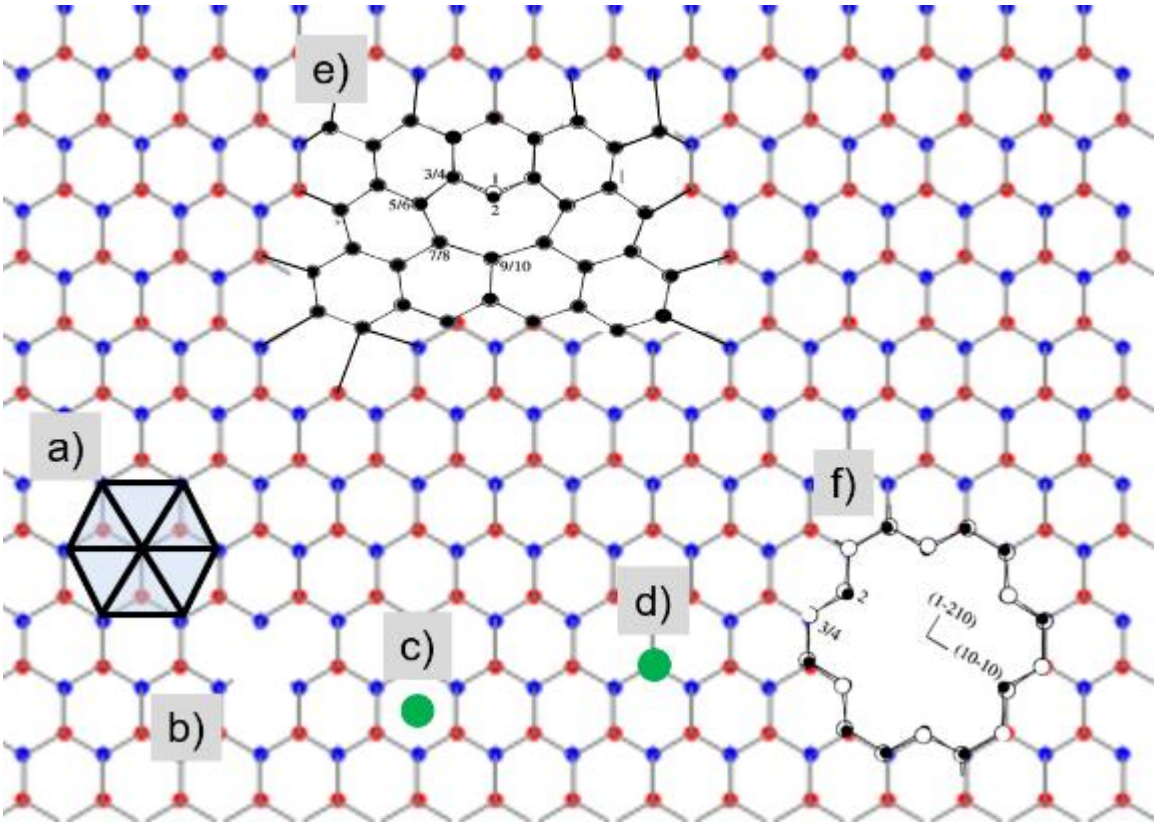


Figure 1: A schematic representation of the (0001) plane of a GaN crystal with a small subset of defects included. a) A reference geometry highlighting the top plane of the Wurtzite unit cell. Schematic representations are included such as b) a vacancy defect, c) an interstitial defect, and d) a substitutional defect. Schematic descriptions of extended, higher-dimensional defects are also included such as e) a closed-core type threading dislocation and f) an open-core "nano-pipe" defect both described by Elsner et al.[23]

Since GaN does not naturally occur on earth, all GaN material today originates from heteroepitaxially grown material that has been plagued by TDs, and these defects have posed a serious problem for III-Ns from the beginning. When growing GaN heteroepitaxially, dislocation form due to both misfit with the substrate and due to 3D growth mode coalescence. The misfit dislocations occur due to lattice mismatch between the epitaxial film and substrate; in order to accommodate the epitaxially grown layer, half planes are formed at the growth interface and result in a residual lattice strain. The crystal system can tolerate such strain

coherently until it reaches a critical thickness or, in the case of large lattice mismatched heteroepitaxy, critical island size[24]. In modern GaN templates grown by MOCVD, these lattice mismatch dislocations are confined to the heteroepitaxial growth interface and do not permeate far into the epitaxial crystal structure. The dislocations observed in these templates originates in the coalescence of the 3D island growths on sapphire surface as shown in **Figure 2**.

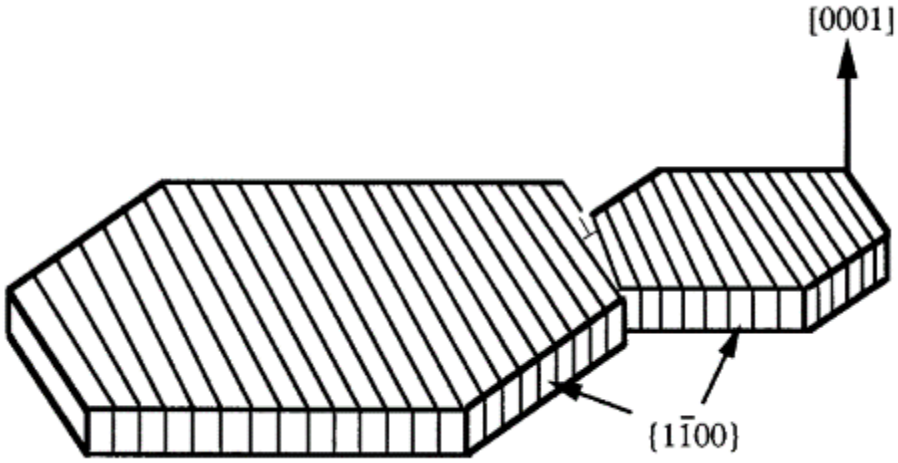


Figure 2: Schematic depiction of island coalescence in GaN heteroepitaxial growth given by Ning et al. (1995).

This dislocation structure in GaN has been extensively studied by high-resolution x-ray diffraction (HRXRD) and transmission electron microscopy (TEM). Edge and mixed-type threading dislocations have been shown to be much more prevalent than their screw-type counterparts, but they all have a line vector within ~10° of the <0001> direction regardless of their Burger's vector, $\vec{\boldsymbol{b}}$ [25,26]**.** Theoretical analyses of TDs in GaN conducted by Elsner et al.[23] have suggested that the dislocation cores in both edge and screw-type dislocations are themselves electrically inactive, however, experimental evidence has shown[27–31] that dislocations have some electrical activity. The best explanation for the electrical activity associated with dislocations in GaN was posited by Arslan and Browning[32] in which they show

by model and experimental verification that there is likely a coalescence of defects (likely V_{Ga}) around the dislocation to relieve the strain induced on the system by the dislocation. These defects are, in contrast, very electrically active with measurable energy levels in the energy band gap[33,34] and are likely the source dislocation-associated charge behaviors.

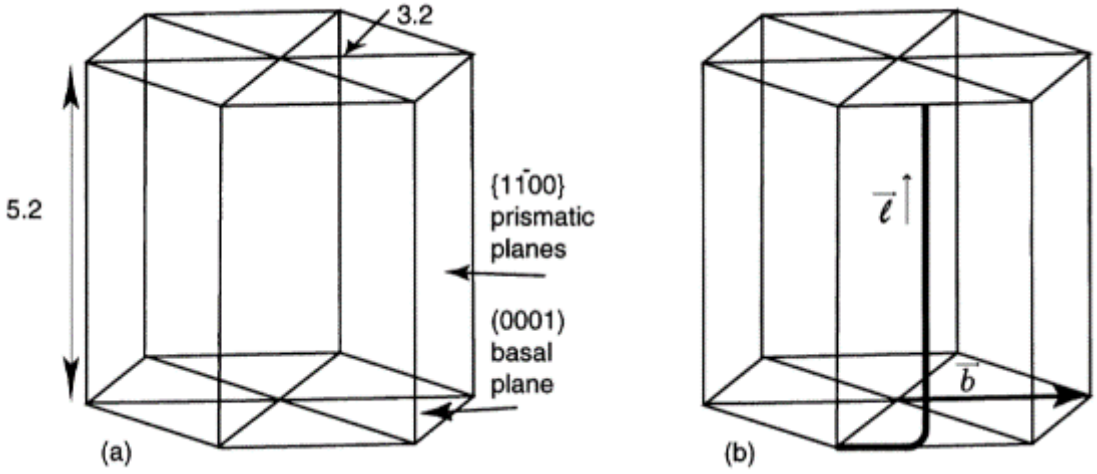


Figure 3: a) The Wurtzite unit cell for GaN with the lattice parameters and plane notations. b) An edge-type dislocation in GaN with a Burger's vector, $\vec{b}$, orthogonal to the line vector, $\vec{l}$[26].

The effect of electrically active TD defects on carrier transport in MBE GaN has been extensively studied and shown that TDs have substantial effects on carrier mobility[30], avalanche breakdown[16], reverse-bias leakage, and reverse-bias breakdown[35]. Despite the high threading dislocation density (TDD) of heteroepitaxial GaN, low-ideality *p-n* junction diodes have been grown with NH_3-MBE with low ideality and reverse bias leakage[36]. Until our work at UCSB, these behavioral observations of GaN p-n junctions had not been explained by theoretical analysis. Our work on this topic is discussed in Chapter 5.

GaN Growth by NH_3-Assisted MBE

All the material in this work is grown on a Veeco 930 Nitride MBE reactor (shown in **Figure 4**). The reactor is tilted at a 30° angle to allow liquid sources to be used in additional cell source ports. The Ga for the growth of GaN is provided by pure Ga metal sources that are heated to > 800 °C to evaporate the pure metal into a coherent molecular beam allowed by the ultra-high vacuum (UHV) environment in the chamber (typically ~ 10^{-9} torr). The N for the growth is provided by a flow of NH_3 regulated by a computer-controlled mass flow controller (MFC), and this NH_3 is then pyrolyzed at the growth surface by the GaN surface (T_{GaN} ~ 800 °C). This source of N constrains growth in two major ways – firstly, the substrate must be hot enough to pyrolyze the NH_3, and the growth of p-GaN is restricted to lower temperature to prevent the formation compensating defect centers or nitrogen vacancies[37]. This means that growth of low temperature materials such as InN is not possible yet in NH_3-MBE, and that p-GaN has a very tight growth window between a high enough temperature to crack the NH_3 and a low enough temperature to prevent the formation of compensating defect complexes.

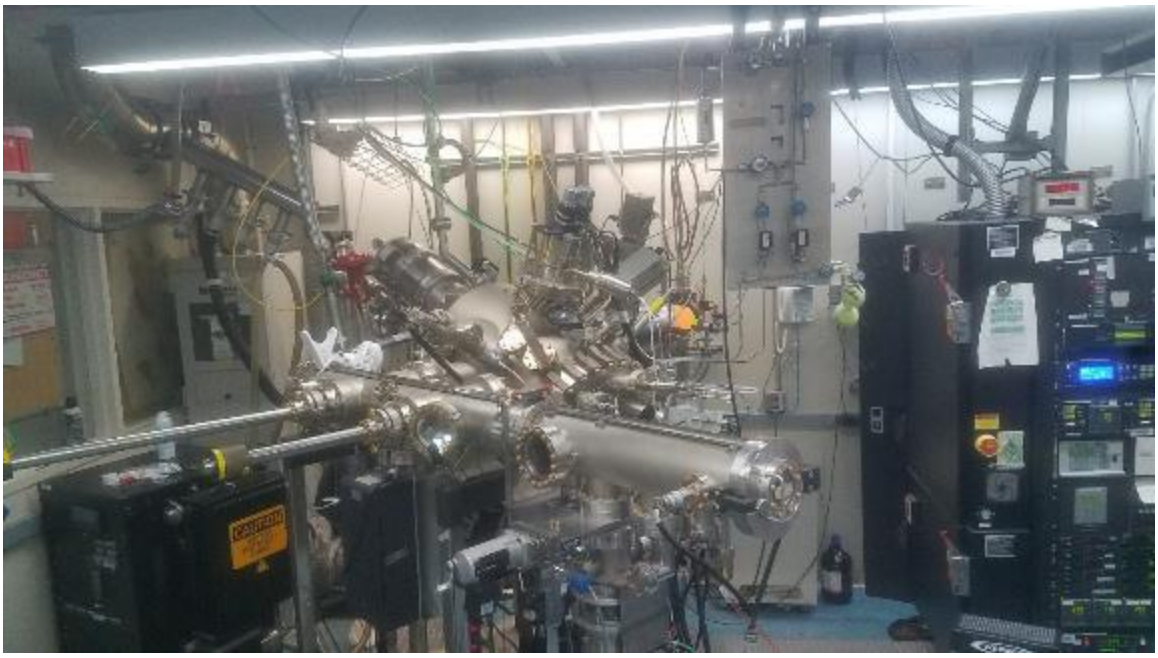


Figure 4: The Veeco 930 Nitride MBE reactor used for this work.

For the most part, NH_3-MBE and MOCVD are similar in that they both face constraints on their growth regimes due to the presence of NH_3 and high temperatures. Most structures and devices can be grown using both since they are both well-established and proven growth techniques, but it is the small differences between the two that dictate which are optimal for a given application. GaN grown by ammonia-assisted molecular beam epitaxy (NH_3-MBE) is used in this work due to ultra-high vacuum standby pressure ($< 10^{-7}$ torr), high-purity sources, and reasonable growth rates (e.g., ~0.5 μm/hr). Vertical power semiconductor devices require thick drift regions and minimal leakage pathways to facilitate high voltages with minimal leakage, thus traditional plasma-assisted MBE (PAMBE) is not suitable for this work. MOCVD, in contrast, has demonstrated much higher growth rates and better vertical electronic devices than PAMBE. However, MOCVD is grown at higher pressures and with metalorganic (MO) precursors, which makes them very robust but with the possibility of high concentrations of point defects such as C and H. Additionally, MOCVD cannot grow active p-type GaN and

requires an additional anneal step to activate the p-GaN by removing the H from the GaN:Mg crystal. This provides significant constraints as to what structures can be grown in MOCVD since the p-type layers of the device cannot be buried in the growth stack. Thus, NH_3-MBE is used to grow structures of reasonable thickness with high quality under growth conditions that are observable and precise. In this growth technique, growth rates of ~450 nm/hr with abrupt interfaces, fine control, and observable morphology can be achieved.

The primary differences between the two growth techniques are the low growth temperature (~820 ° C), pure sources, and ultra-high vacuum environment of NH_3-MBE. These qualities make NH_3-MBE much easier to observe *in situ* making it an ideal research growth technique since *in situ* measurements such as reflection high energy electron diffraction (RHEED), can be used to track the growth surface in real time. These qualities also give MBE a degree of theoretical simplicity – rather than requiring dissociation of metalorganics and gas flow calculations, NH_3-MBE simply requires vaporization of pure source material in a vacuum for deposition. There are much fewer carbon contaminants, no metalorganic pyrolysis, and no growth chamber gas flow management required for NH_3-MBE, thus it is ideal for thin crystal regrowth and for creating high electron mobility GaN layers.

There are two methods of MBE used in GaN growth – plasma-assisted MBE (PAMBE) and ammonia-assisted MBE (NH_3-MBE). The nominal difference between these two techniques is the source of growth nitrogen – PAMBE uses a controlled N-plasma to supply monoatomic nitrogen for crystal growth while NH_3-MBE uses ammonia cracking (T_C = 430 °C) much like MOCVD to supply nitrogen. This results in a substantial difference in details between the two methods since PAMBE generally occurs in a Ga-rich environment while NH_3-MBE occurs in an N-rich environment (V/III ~ 1,000). In the N-rich environment, growth

occurs with the ammonia pyrolysis adsorbing N onto the surface of the substrate where the flux of Ga then controls the growth rate; however, this then leaves free H and H_2 in the system that can then form Mg-H complexes if growth at high temperature (> 750° C). In the Ga-rich environment in PAMBE, a chemisorbed adlayer forms that promotes the migration of N and realize smooth step-flow growth. When the Ga flux is too high, in addition to the Ga adlayer, Ga droplets form on the surface. The droplets result in poor morphology. To counter this tendency, PAMBE cycles the flux of N plasma to allow the Ga droplets to desorb from the surface and allow GaN growth without 3D Ga defects. Even without the formation of Ga droplet leakage paths, theoretical analyses of TD formation in a Ga-rich environment indicate TDs formed under these conditions will be decorated with Ga metal thereby causing them to very leaky. However, there are no post-adsorption remnants making PAMBE material extremely pure.

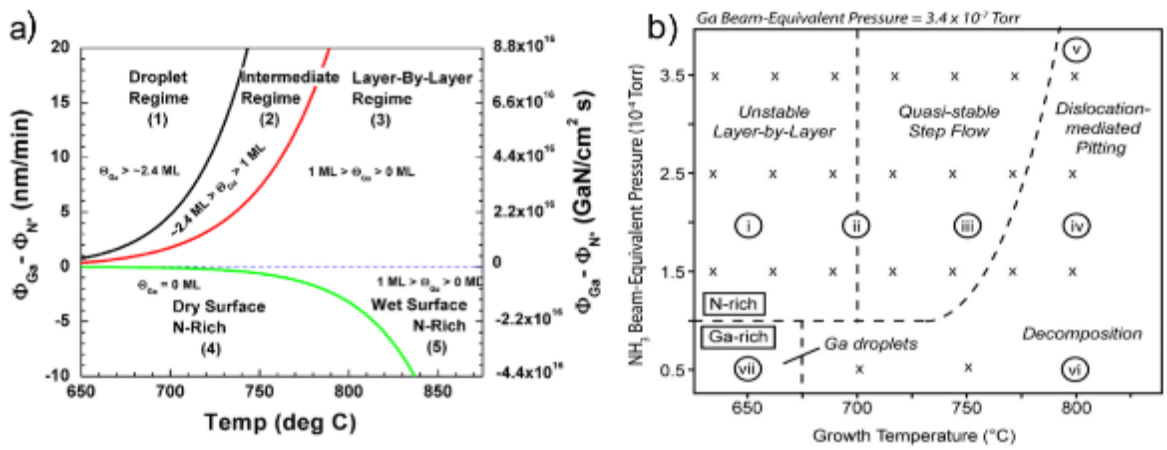


Figure 5: Growth maps for a) PAMBE and b) NH_3-MBE. Note that the growth regime for good NH_3-MBE (quasi-stable step flow growth) is much larger than growth regimes for PAMBE (intermediate and stoichiometric).

In general, NH_3-MBE has been preferred for vertical device fabrication since its growth regimes are not as strict and do not result in metal-rich defects (i.e. droplets and TDs) forming during growth. These droplets provide current conduction paths through the grown structure

that can cause leakage and breakdown. However, PAMBE growth generally results in higher quality crystal structures and does not require working with ammonia. Ammonia is not only toxic but also forms ammonia ice on the liquid nitrogen cooled cryopanel components of the MBE system. This ice can accumulate lethal levels of frozen NH_3 within the chamber that can be rapidly released in the event of a cryo-system failures making regular de-icing regimes (called Ammonia Recoveries) a safety requirement for NH_3-MBE systems.

For these strengths, however, MBE falls short to MOCVD on two fronts – the growth rate is typically slower, and the incorporation of O impurities are more prevalent. However, recent research by McSkimming et al.[38] has demonstrated growth rates up to 7.6μm/hr using high N-flux PAMBE with controlled doping and has great promise for future research and application if crystal and stoichiometric quality can be improved. However, typical growth speeds for NH_3-MBE are generally around 100-500 nm/hr, but growth rates of up to 2μm/hr have been achieved on the system with good crystal quality. However, such growth rates rapidly deplete the metal sources in the system making system openings more frequent. These factors make the formation of nucleation layers more difficult as thick layers and higher temperatures are ideal for GaN nucleation to grow material with TDD < 10^{10} cm^{-2}. Additionally, it has been observed that optoelectronics grown by MBE seem to fall substantially short of their MOCVD counterparts for reasons that are still poorly understood, but likely associated with an unacceptable concentration of strong nonradiative recombination centers, including calcium in MBE materials.

Chapter 2. Growth

Substrate Characterization

When receiving a new shipment of samples, non-destructive characterization should always be done to ensure sample quality. For most of this work, new substrates underwent high-resolution X-ray diffraction (HRXRD), cathodoluminescence (CL), and atomic force microscopy (AFM). HRXRD probed the internal crystal quality of the substrate by using the rocking configuration of the Panalytical HRXRD tools to measure the FWHM of the substrates' (0002) and (202-1) planes. These planes provide information on the defects affecting the c-plane periodicity and a+c-plane periodicity, respectively.

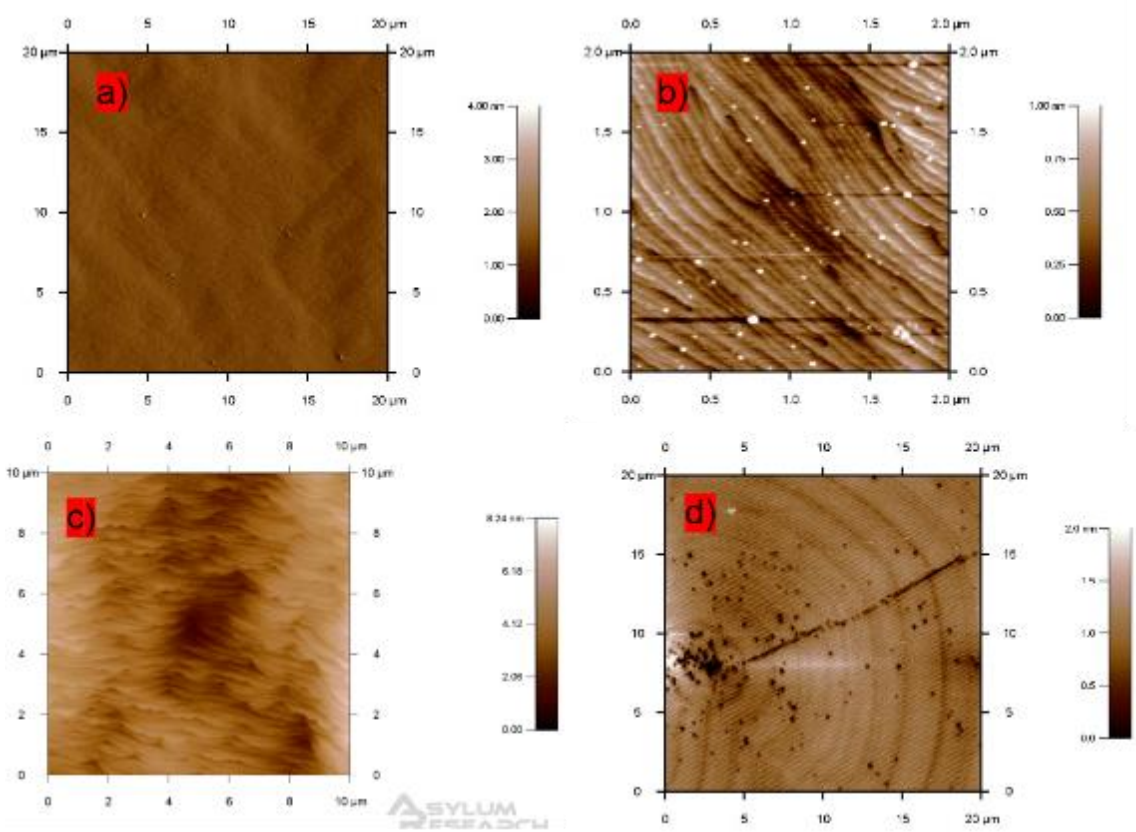


Figure 6: a) – c) show pre-growth terraced steps suitable for MBE growth. d) A substrate surface with many pit defects associated with threading dislocations terminating at the surface. This growth surface will not produce high quality

epitaxial thin films in MBE due to these morphological defects at the growth surface.

Atomic force microscopy (AFM) is the first characterization method utilized for new samples. Typical high-quality AFM micrographs are given in Figure 6 a) – c). The most important features to observe in this characterization are the presence of well-defined steps and terraces and low concentrations of morphological defects such as pits. In Figure 6a), a large-scale AFM micrograph ($20\mu m$) is given with a low concentration of surface defects such as pits or clusters. In Figure 6b) and c), AFM micrographs of small dimension are shown of different substrates with clear step-edges (note that in Figure 6b), the white dots are dust particles due to the N_2 gun being down). Finally, in Figure 6d), an AFM micrograph of a bad substrate demonstrates what a poor substrate surface looks like with a high concentration of surface defects and clustering.

High-resolution x-ray diffraction (HRXRD) can also be used to assess the quality of substrates periodic crystal structure to non-destructively characterize various aspects of crystal quality. To get a holistic understanding of the crystal structure, ω – rocking curve scans must be conducted for the (0002) and $(10\bar{1}2)$ (or any other off-axis reflection (hkl) with h or k ≠ 0) reflections reflections, where the off-axis $(hk.l)$ reflection must be measured in a skew symmetric geometry. These two points provide information on the edge-type dislocations and all dislocations, respectively. Distortions with an $\vec{a}$ and $\vec{c}$ component Burgers vector will broaden the (0002) and $(hk.l)$ directions will cause broadening of these peaks; by conducting this scan, one can obtain a general comparison in crystal quality between substrates. Measured characteristics are given in Table 3 for common substrates.

	(002) FWHM (ARCSEC)	(102) FWHM (ARCSEC)
GAN-ON-SAPPHIRE	327	353
FS N-TYPE	115	37
FS SEMI-INSULATING	142	60

Table 3: Typical measured HRXRD characteristics for common substrates used in MBE growth.

Lastly, cathodoluminescence (CL) can be used to visually confirm the threading dislocation specifically for both n- and p-type GaN[37]. By bombarding the substrate with electrons in a scanning electron microscope, photons are generated within the crystal, and these photons either escape the crystal to be measured by our Gatan CL tool or are rapidly recombined at threading dislocations which act as recombination centers for photons. This causes threading dislocations to be appear as black spots among the areas of high photon emission in the crystal as shown in Figure 7. It is highly recommended that these spots be counted using a counting software rather than by eye for both the sake of accuracy and convenience.

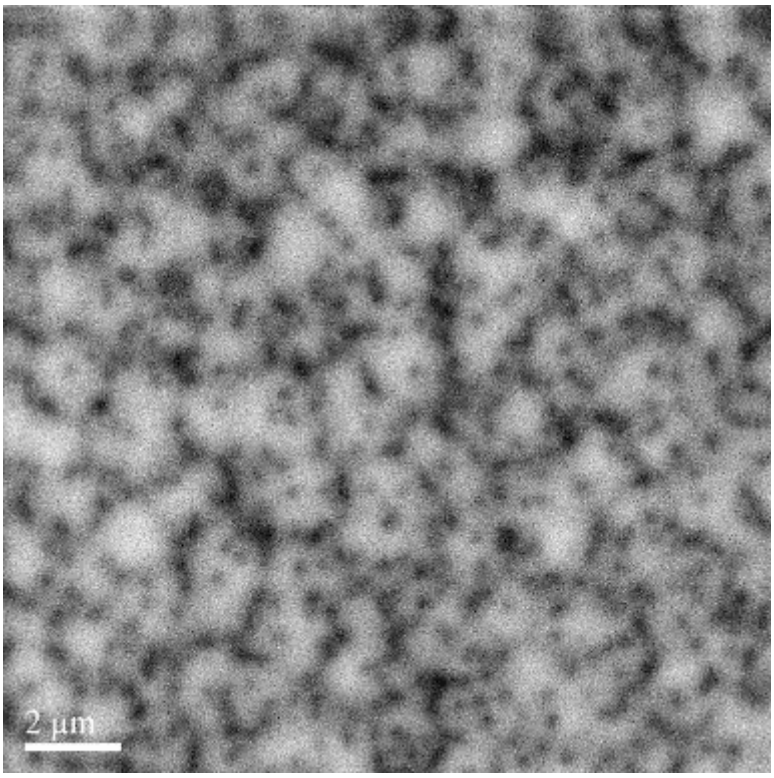


Figure 7: CL image of GaN-on-Sapphire substrate with a threading dislocation density of $\mathbf{3 \times 10^{8}\ cm^{-2}}$.

Growth Preparation

Prior to growth, 2" wafers are degreased with a thorough solvent clean and loaded into an electron beam (e-beam) deposition chamber. A 5/ 500/100nm Ti/Pd/Ti metal stack was deposited on the back surface. This stack was optimized for radiative heat transfer in the MBE system as well as to facilitate the measurement of measured sample temperature stability in high temperature NH_3 environments. The process by which this metal stack was reached is discussed in the Appendices. The wafers were then diced into 1 cm × 1 cm samples using an ADT Dicing Saw and UV-release adhesive. The wafers were then checked with atomic force microscopy (AFM) to ensure that the surface had a terraced surface suitable for achieving step flow growth modes in MBE (Figure 6).

All samples entering the MBE system were cleaned using a standard solvent procedure (5' acetone, 5' methanol, 5' isopropanol under high power sonication). The sample was then loaded into the MBE system's entry / exit chamber (10^{-8} torr < P_{EE} < 770 torr) on a growth block where it is baked at 160 °C for 2 hours to evaporate any water or loose contaminates on the surface of the block or sample. The block was then transferred into the buffer chamber (10^{-9} < P_{BC} < 2×10^{-6} torr) where it is baked at 400 °C for 1 hour. After completion of the bake and stabilization of the buffer chamber pressure, the block was transferred into the main growth chamber (9×10^{-9} torr < P_{GC} < 5×10^{-5} torr). Full details on the loading and growth preparation procedure can be found in the Appendices.

Typical Calibration Procedures

Emissivity Calibration

Before growing actual samples, an emissivity calibration must be conducted to assure *precise* (not necessarily accurate) measurement of surface temperature from substrate to substrate. This calibration was done by taking a diced 1 cm × 1 cm sample (typically a non-square sample since those are less useful for devices and growth science) and coating it with 500 nm of Al using E-Beam #3 (Temescal). The Al strip was used as an indicator of the surface temperature as the Al with transition from a smooth to balled surface when the Al melts due to the high interface energy; this transition results in the visual appearance of the Al strip from shiny to matte.

The calibration sample was then cleaned and loaded as described in the previous section and loaded into the main chamber. This part of the calibration process was substantially easier and more reliable with at least two growers present – one to adjust temperature parameters and the other to monitor the substrate surface. With the sample surface easily visible from the MC

loading viewport, the substrate temperature was then increased to 650 °C (just below the Al melting point of 660 °C) with a slow ramp rate of ~30 °C/min to prevent overshoot of the substrate heater temperature. Once the temperature is near the melting point of Al, it is essential that the ramp rate be substantially reduced. The best calibration results (measured by clarity of transition between Al phases) were realized when the substrate ramp rate was reduced to 5 °C/min, temperature increases were done in 5 °C intervals, and was allowed ~5 minutes to settle. If these precautions were not taken, the metal may heat unevenly, or the melting point may be passed entirely thereby reducing the accuracy of the calibration.

Once the Al transitions to a matte appearance, the substrate then needed to be rotated to face the pyrometer. The pyrometer then needs to probe the sample away from the Al strip; the second grower for the calibration then needs to adjust the emissivity parameter of the pyrometer controller until the read temperature is 660 °C. This emissivity then needs to be logged in the growth log.

It is important to note that this emissivity is not a measurement of the material emissivity and should be treated as its own value and not compared with literature emissivity values. It is important to understand that although the backside metal is being probed – substrate interface, it is being calibrated with respect to the surface temperature. This means that although two substrates may have the exact same optical properties, differences in their thermal properties will result in different calibrated emissivities (as is the case for GaN-on-Sapphire and FS GaN).

Growth Rate Calibration

A basic requirement of epitaxial growth is fine control of epitaxial layer thickness, and to achieve that, growth rate calibrations must be done before electronic structures can be grown. To calibrate the growth rate associated with a Ga flux from a cell, we grew calibration growths

in which we could measure the thickness of a grown layer using thickness fringes observed in HRXRD $\omega - 2\theta$ scans of (002) peak. To observe thickness fringes, a contrast layer is required to observe the contrast between the crystalline periodicity and the thin calibration layer grown. This is generally done by growing a very thin AlGaN layer (Open Shutter Time: 2') followed by a thin layer of GaN (Open Shutter Time: 15'). Once the sample has been grown and scanned by HRXRD, the periodicity of the thickness fringes can then be used to calculate the thickness of the 15' GaN layer on top the structure. From this thickness, the growth rate in nm/hr can be easily calculated.

Doping Calibrations, Part 1: SIMS Structures

Doping calibrations are essential for all structures that require control of carrier type and concentration. For instance, Hall structures (discussed in the next subsection) probe the electronic carrier properties, but these properties assume an incorporation of dopants. If a doping source is depleted or damaged in some way, a SIMS stack can quickly provide this information without being convoluted with the growth condition dependencies inherent in Hall measurements. In these structures, a stack of growth is done with layers at different doping conditions separated by a thin marker layer with good contrast to the doping layers. Typical marker layers are 10 nm of AlGaN; InGaN can also be used but the marker peaks are substantially lower than AlGaN due to the poor incorporation of In at typical growth conditions. The doping layers are typically anywhere from 100 to 200 nm with the thickness dependent on the growth rate and quality. Slow growth rates necessitate thinner layers to keep growth times reasonable, but thinner layers are more subject to poor contrast imposed by an etch surface roughness and sidewall that cause other layers to interfere with the layer of interest.

Once grown, the samples are then analyzed using secondary ion mass spectroscopy (SIMS) to evaluate the dopant (not carrier) concentration in the crystal. A typical SIMS stack scan is shown in **Figure 8** showing the temperature dependence of the Si concentration in the GaN crystal and **Figure 9** showing the variation in Mg and atmospheric incorporation with growth condition. In addition to gaining insight regarding the dopant concentration, SIMS stacks can also be used to observe the dependence of atmospheric and unintentional impurity incorporation at different growth conditions.

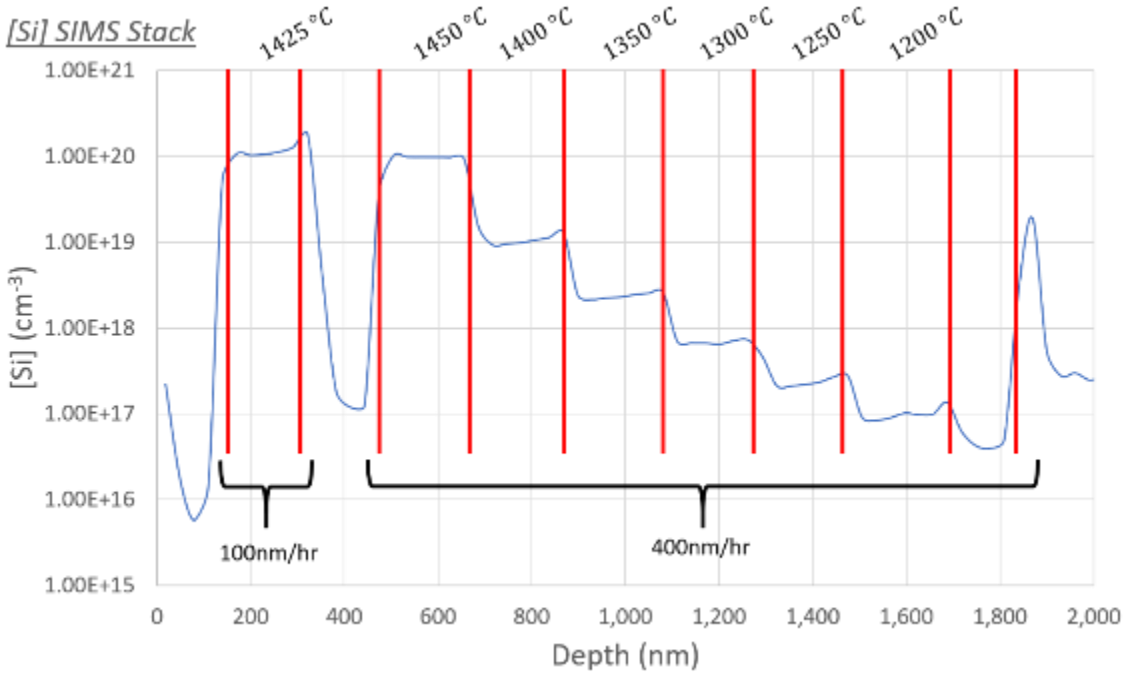


Figure 8: Si SIMS stack demonstrating typical calibration results necessary when growing electronic devices. Note that in the top layer of the SIMS structure, the growth rate is reduced from 400 to 100 nm/hr by reducing the Ga cell temperature. During this period, the substrate accumulates contaminants from the environment that result in the small spike in Si concentration at that interface.

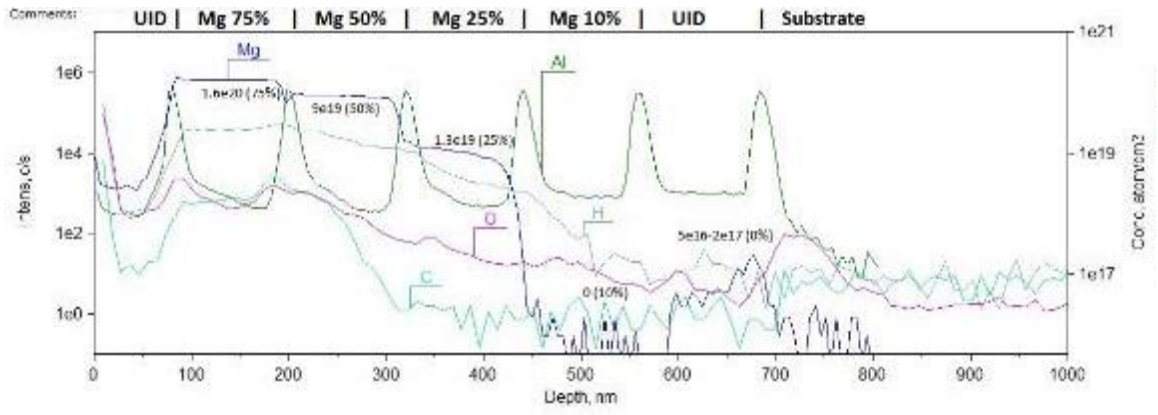


Figure 9: Mg SIMS stack showing both typical dopant incorporation for variable valve openings as well as atmospheric incorporation at high Mg concentration.

Doping Calibrations, Part 2: Hall Structures

Once dopant incorporation is confirmed via SIMS, the last calibration necessary is the growth and characterization of Hall Effect structures to confirm the electronic activity of the growth condition. A Hall sample must have adequate thickness such that impurities at the regrowth interface have a minimal impact on the measurement; usually 300 nm is adequate, but 500 nm to 1 μm is more accurate. The Hall sample must be grown at the same growth condition as the correlating SIMS growth in order to provide the most accurate assessment of the electronic crystal qualities. Typically, these calibration samples are measured by placing large In dots on the corners of the samples and measuring the sample in a simple Van der Pauw configuration; by using large In dots, the effect of the Schottky contact interface with the metal can be minimized to form a pseudo-Ohmic. This Ohmic behavior must be observed prior to conducting the Hall measurement to ensure that the result is not convoluted with a depletion region variation associated with a measurable Schottky interface.

This step is particularly essential in determining the proper growth condition of p-type GaN since Mg activation and defect formation must be balanced to achieve hole conductivity.

GaN:Mg material grown below 720 °C will have good hole activation but will be plagued by low mobility carriers due to a high concentration of defects. Additionally, p-GaN grown at this cold growth condition will also be characterized by a high pit density as the Mg mediates defect formation and the growth regime slides into an unstable layer-by-layer growth mode[39]. A sample micrograph of such a surface is presented in **Figure 10**.

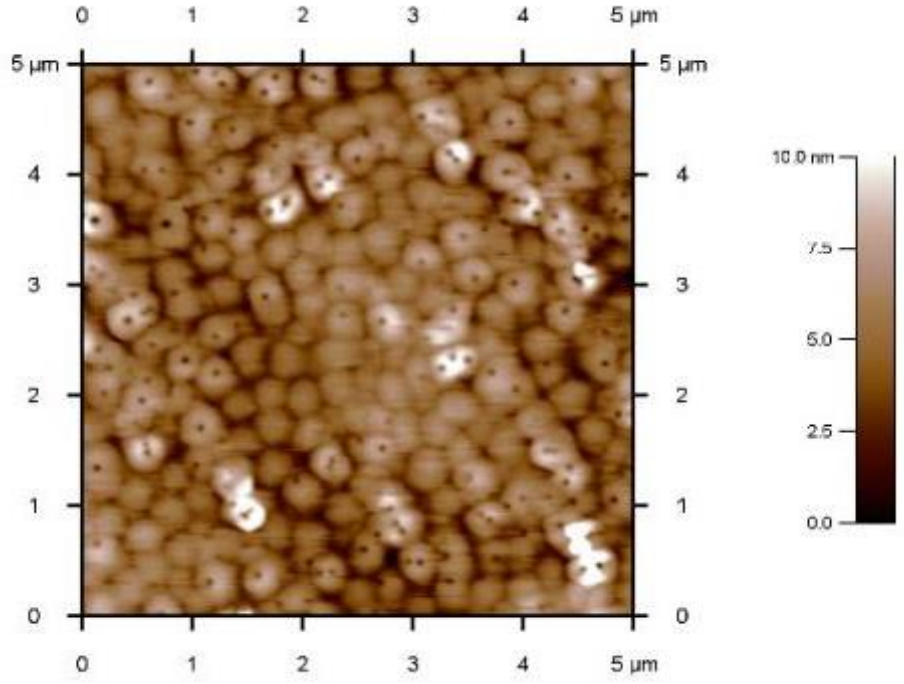


Figure 10: AFM micrograph showing pit formation at temperatures below the optimal growth temperature of p-GaN.

These pits have depths that are unmeasurable by AFM scans but can have depths greater than 60 nm. However, material grown above 750 °C has extremely poor hole activation even at 760 °C due to the formation of compensating centers and defects[37] in the NH_3 growth environment. Thus, good p-GaN must be grown within these growth conditions with the best material being grown at 750 °C. This growth condition does result in slightly reduced hole conductivity but has no surface pits that were found to correlate with leakage currents in our

p-n diodes. This behavior can be clearly seen in **Table 4** where p-GaN calibrations were conducted on a stable backside metal.

Dopant Control	50%	50%	50%	50% + In
T_{sub} (°C)	900	880	860	860
n / p (cm^{-3})	1.7e17	2.6e17	1.4e18	1.0e18
μ_n (cm^2 / V-s)	4.1	10.0	5.3	10.4
R_{sh} (Ω/ □)	289,900	66,000	28,000	19,400
ρ (Ω - cm)	9.0	2.5	0.81	0.58

Table 4: Dependence of p-GaN properties on growth conditions. Note that the hole concentration drops markedly for growth temperatures higher than 860 °C. Furthermore, it should be noted that, without any optimization or specialized growth structure, notably high-quality p-GaN was grown.

Defect Control

One of the major barriers in assessing the effects of defects on carrier transport has been the lack of controllability in defect concentrations. Some studies have been conducted using different substrate types to controllably vary threading dislocation density and such research is presented in Chapter 4. By growing identical structures on substrates of different threading dislocation density, the effect of these defects on the transport can be measured, compared, and analyzed. This methodology has provided valuable insight into the empirical effects of dislocations on carrier transport in various devices.

Additionally, it has been recently discovered[40] that MBE material around the world has significant and unintentional concentrations of calcium. In MBE, this calcium impurity originates at the growth surface of the substrate; some of these surface impurities incorporate into the growth layers (at low temperature) while the remaining adatoms ride the surface. The origin of these impurities is not certain, but it is likely due either to chemical-mechanical

polishing (CMP) or ambient contamination. Additionally, a means of systematically reducing the concentration of this point defect has also been pioneered. This presents an opportunity to observe the effects of these point defects on the behavior of *p-n* junction diodes grown by NH_3-MBE as outlined in this work.

By utilizing the temperature-dependent incorporation rate of surface Ca, the concentration of these point defects can be varied in a controlled and consistent manner as shown by Young et al[40]. The Ca appears to spike layers grown at low temperature, thus in order to reduce the concentration of the Ca in a device structure, one can capture the Ca in layers grown at low temperature. Ca incorporation into GaN during growth is inversely dependent on temperature with low temperature regions (i.e. InGaN) having significantly higher Ca incorporation than the high temperature regions (i.e. n-GaN). To reduce Ca concentration in active areas such quantum wells (QWs) and junctions, a low-temperature (LT) InGaN/high temperature (HT) GaN superlattice is grown to incorporate Ca from the growth surface into an unused region. The low-temperature InGaN regions absorb Ca from the surface while the high temperature GaN regions are used to smooth surface roughening caused by LT growth. LT InGaN totaling ~50 nm thickness over the course of 10 periods resulted in three orders of magnitude reduction of Ca defects as shown in **Figure 11**. Using this methodology, the study of point defects like Ca on the behavior of devices grown by MBE can be studied in a controlled fashion.

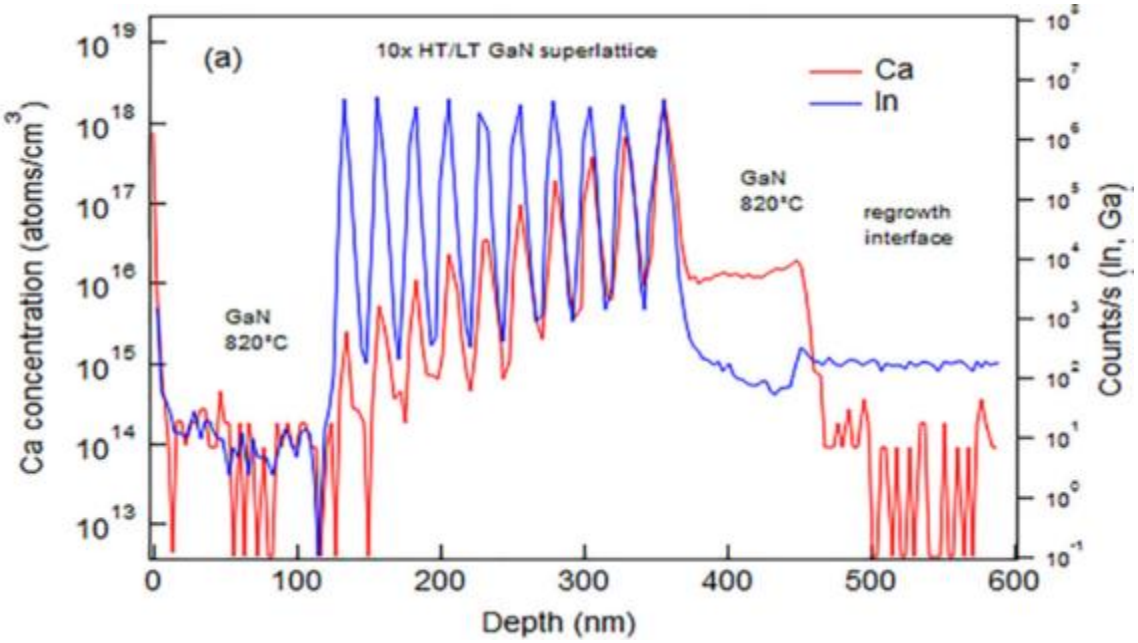


Figure 11: SIMS analysis of Ca reduction superlattice structure presented by Young et al.[40]. Note that the Ca concentration spikes in the low temperature InGaN regions, but the spikes decrease in severity with each InGaN layer.

p-n Junction Diodes

In this work, a p-n diode structure was grown to study the effects of both Ca point defects and threading dislocation density on the transport properties of GaN vertical devices. This structure is shown in **Figure 12** and was built off the work of my predecessor, Dr. Christoph Hurni[36].

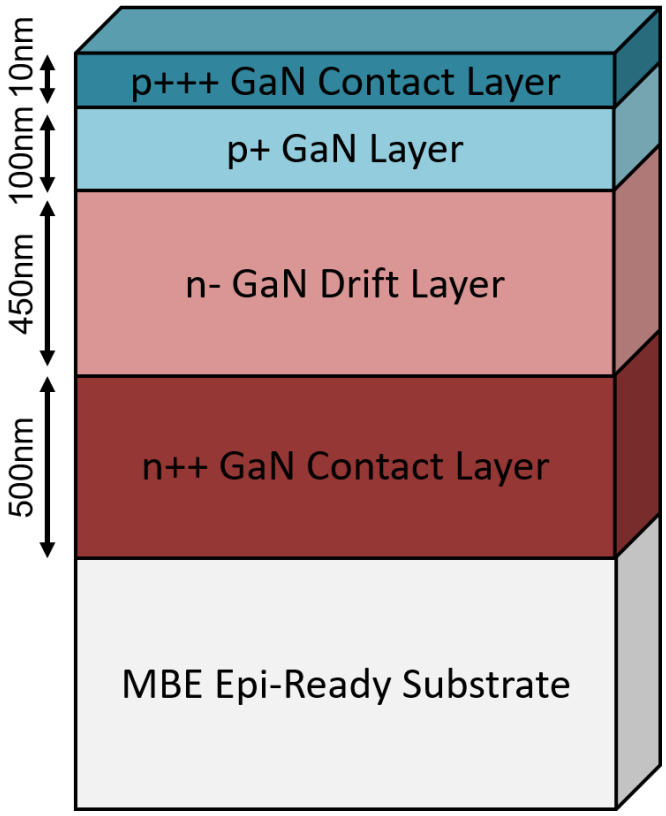


Figure 12: The typical p-n diode structure grown for both experimental studies in this work.

A thick 500nm n++ contact region was grown to provide a large range in which the etch can finish and still form a proper n-contact. The 450nm n- region allows the electric field in the device to held over a thicker layer to avoid the premature breakdown of the material. The p-layer has a high concentration of Mg, but Mg is a deep acceptor in GaN thus only has an ~1% activation rate, so this density is necessary to form conductive p-GaN. This high concentration of Mg also means that space charge region is located mostly within the n-layer (Mg:Si ~ 100:1) which allows for the simplification of calculations regarding breakdown fields. Finally, a thin, heavily doped p^{++} contact region is grown to facilitate the formation of Ohmic p-contacts.

For the contact regions, extremely high doping is necessary to form low resistance contacts. For the n-contact region, good pseudo-Ohmic contacts can be formed with concentrations as

low as $5 \times 10^{18}\ cm^{-3}$, but doping concentrations of $10^{20}\ cm^{-3}$ produce the best contacts. p-GaN contacts, however, have much more stringent growth requirements. To form good, pseudo-Ohmic contacts, $[Mg] > 3 \times 10^{20}\ cm^{-3}$ is necessary. If the doping is lower than this, non-linear contact behaviors arise. In addition, this high doping concentration also restricts the thickness of p-GaN contact layers as these growths generally result in poor quality material with various defects and inversion domains. Furthermore, as will be discussed in 0. Chapter 3. Processing, p-contacts are *very* sensitive various processing procedures such as organic contamination by photoresist, ambient contamination of the contact interface, and ultra-sonic damage to the contact interface. They cannot be exposed to photoresist nor can the sample be sonicated once the p-contact metal is down. Both will result in poor performance as characterized by rectifying behavior.

To calculate the necessary drift thickness for the p-n structure, one simply needs to combine the following equations

$$W_D = \sqrt{\frac{2\varepsilon}{q}(N_A^{-1} + N_D^{-1})(\phi_{bi} - V_a)} \tag{3}$$

$$V_a = -V_{br} = 60\left(\frac{E_g}{1.1}\right)^{1.5}\left(\frac{N_D}{10^{16}}\right)^{-0.75}. \tag{4}$$

where W_D is the depletion width, ε is the material permittivity, q is the electron charge, N_A is the concentration of acceptor dopants, N_D is the concentration of donor dopants, ϕ_{bi} is the built-in potential of the junction, V_a is the applied bias, V_{br} is the breakdown voltage, and E_g is the band gap energy. Note that Equation 3 only includes the depletion region on the n-type side of the *p-n* junction. This model assumes a lightly-doped n-type side in the junction, thus the region with the largest depletion will be this side of the junction. By making this assumption

in this model, we can simply the calculations required without losing any practical experimental options since lightly-doped p-GaN is rarely used in devices. By utilizing the model in Equation (4) presented by Sze & Gibbons[41] and combining it with the depletion width on the lightly doped, n-type side of the junction, the necessary thickness to observe breakdown can be calculated. For this work, drift thicknesses at least twice the needed thickness were used.

Chapter 3. Processing

After samples are grown, they must then be fabricated into vertical p-n diodes in the Class 100 Nanofabrication facility. The final process used for devices was the result of troubleshooting and optimization efforts that are outlined in this chapter.

Process Flow

In the interest in maintaining the integrity of the p-contact while mitigating sidewall leakage, the "Passivation" process deposits SiO_2 on the clean p++ surface to protect it from contamination. This process flow is diagrammed in **Figure 13**.

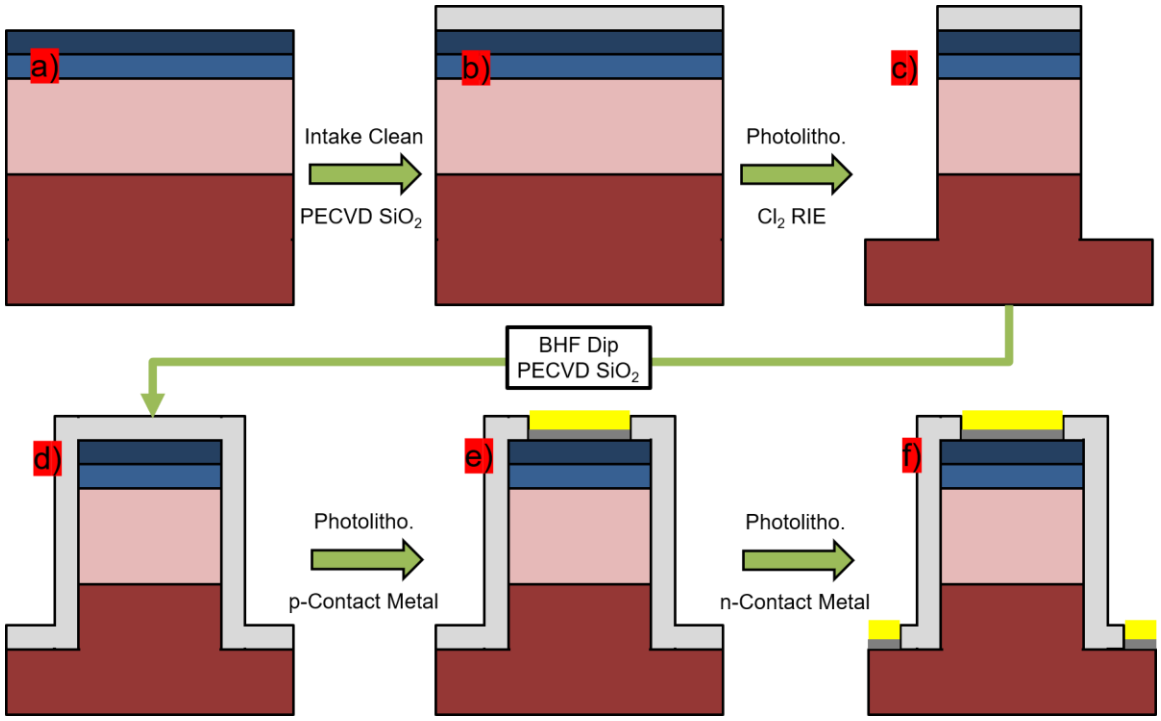


Figure 13: Passivation process flow diagram. a) Bare epi. b) SiO_2 deposited on epi surface after intake clean. c) Isolation mesa by RIE Cl_2 dry etching. d) Conformal coating of SiO2 for sidewall passivation. e) p-contact deposition by e-beam #3 f) n-contact deposition by e-beam.

This fabrication process begins similarly to the "Metal First" process discussed in Appendix A with an intake solvent clean followed by an HCl dip. However, since SiO_2 is being

deposited on the surface, the removal of suboxides at the surface was done by immersing the sample in Buffered HF (BHF) for > 10'. After the sample had been immersed in BHF, it is then immediately transferred to a PlasmaTherm plasma enhanced chemical vapor deposition (PECVD) chamber where 50 nm of SiO_2 was coated onto the surface. 50 nm was experimentally determined to be the ideal oxide thickness due to the optimization of two opposing factors. First, if the oxide was too thin (< 50 nm), it would fail to protect the p-GaN surface which resulted in poor contact quality. However, if the oxide was too thick (> 100 nm), then the BHF dips used to selectively remove the oxide would not remove the material uniformly leaving some oxide on the surface that is visible under optical microscopy. This oxide was very difficult to remove and was usually removed at the cost of smaller features such as the circular TLM (cTLM) rings.

The mesa patterning step immediately followed the oxide deposition. nLoF-2020 was used as in the "Metal First" process, but exposure times needed to be lengthened substantially from 10" to 14" which was likely due to both aging of the UV lamp and the i-line filter necessary for this photoresist (PR). Patterning was followed by a 30" O_2 plasma clean to clean up smaller features in preparation for the oxide removal. Etch rate calibrations of the SiO_2 in BHF were conducted using control samples with thicknesses measured by ellipsometry – the etch rate was determined to be ~ 400 nm/min. To ensure complete removal of the surface oxide, samples were immersed in BHF for 60" which was always sufficient to remove a 50 nm layer of SiO_2.

The samples then underwent RIE processing as previously discussed, and the PR and oxide were then stripped from the surface using AZ NMP Rinse at 80 °C and BHF dips, respectively. It is important to allow the PR stripping step enough time to completely remove the PR from the surface (usually 4 – 8 hours) – failure to do so results in residual PR that is not entirely

removed during the oxide removal steps and results in poor quality devices. After the PR is removed from the surface, the sample can then be immersed in BHF in preparation for a second conformal coating of 50 nm SiO_2 by PECVD. This oxide layer will both protect the p-GaN surface and passivate the sidewalls from damage and contamination.

From this point, the deposition of contact metals occurs in much the same way that it did in the metal first processing. The only noteworthy differences are that the p-contacts are patterned rather than etched, and the protective oxide must be removed by a 60" BHF dip prior to metallization. This removal also acts to clean the surface of any contaminants and forms very good contact surfaces and properties.

Electrical Verification

Samples processed with this method were also electrically tested to confirm that the sidewall leakage and 1D normalization behavior had been eliminated (Figure 14). The final process resulted in good areal normalization of the current over the device indicating that previously observed issues with linear normalization had been resolved by this process. This process was the final flow that was used to fabricate diodes for this work.

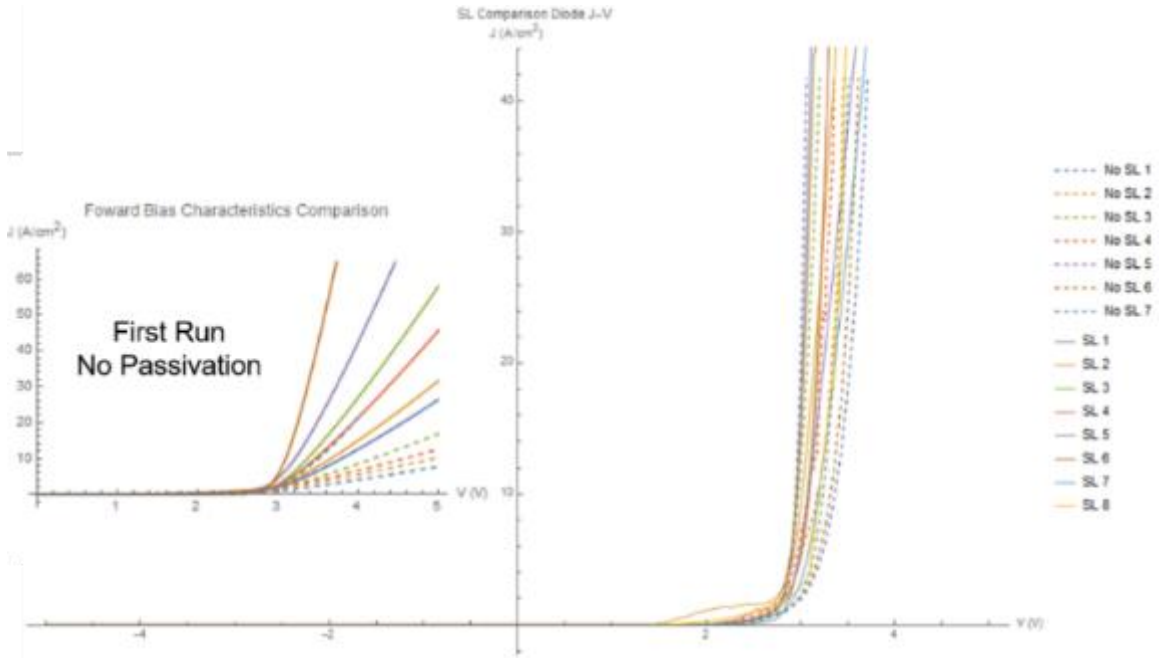


Figure 14: Comparison of "Metal First" and "Passivation" diodes demonstrating the elimination of parasitic sidewall leakage and normalized areal distribution of current. Note that in the inset, the devices with the smaller areas (a.k.a. a high perimeter-to-area ratio) exhibited substantially higher current densities than in the devices with no parasitic pathways as would be expected.

Processing Effects Summary & Optimization Notes

By utilizing an SiO_2 passivation process to protect the sidewalls and p-GaN surface, issues found during an initial process flow involving blanket p-GaN metal deposition (Appendix A: Processing Optimization) were solved. The “Metal First” process results in substantially leakier diodes with extremely high current densities in devices with a high perimeter-to-area ratio and were better normalized to 1D current distribution rather than a 2D one. This effect is suspected to be due to the migration of metals from the p-contact to the sidewall during the mesa etching process although other factors such as older chamber treatment recipes could have also been responsible for these leakage mechanisms. Although this conjecture was not tested in depth, the elimination of non-areal leakage current with the addition of SiO_2 passivation solved the problem without need for further analysis.

Similarly, the effect of the dry etch rate was also studied. Two identical samples were processed using the "Passivation" flow with two different etches – the standard 100 W Cl_2 etch (~75 nm/min) and a 200 W $SiCl_4$ (~30 nm/min). The lower etch rate resulted in substantially leakier diodes. This result led to the conclusion that, in accordance with our prior suspicion of Au migration, the Ti remaining on the backside of the samples may also be contributing to sidewall leakage. If this were the case, the longer etch time would result in a leakier device as was observed. Further optimization of this process could potentially explore the effects of backside metal removal on the overall device quality, but it was not explored in this work.

Lastly, exposure of the sidewalls to plasma damaged induced by the PECVD for passivating SiO_2 was explored as a source of potential optimization. Devices with atomic layer deposition (ALD) layers of 25 nm Al_2O_3 were fabricated. The thin layer of Al_2O_3 was chosen solely due to the time constraints on the ALD tool in the cleanroom. It was found that this process led to poor p-contact characteristics including non-Ohmic behaviors. This behavior was attributed to the small thickness of the oxide resulting in poor protection of the p-GaN surface.

Chapter 4. Defect Characterization

Calcium Point Defects

Introduction

The first project pursued in the study of defect mediated transport in *p-n* diodes centered on a new discovered point defect in MBE grown material: Ca impurities. Recently, it has been discovered that MBE material around the world has significant and unintentional concentrations of calcium[40]. Additionally, a means of systematically reducing the concentration of this point defect has also been pioneered by Young et al. This presents an opportunity to observe the effects of these point defects on the behavior of *p-n* junction diodes grown by NH_3-MBE since these point defects can be systematically controlled by growth conditions.

Theory work by Shen et al.[42] has predicted that Ca in the III-N material system acts as a compensating point defect. Their calculations predict (**Figure 15**) that Ca will preferentially occupy different lattice sites based on the Fermi energy of the system. Ca in n-type GaN is predicted to be a substitutional point defect on the Ga site, Ca_{Ga} while it should be an interstitial point defect, Ca_i, in p-type GaN. Furthermore, a Ca_{Ga} point defect is predicted to act as a deep acceptor in n-type material (Fermi level close to the conduction band) while the Ca_i point defects are predicted to act as shallow double donors when the Fermi level is close to the valence band. This theoretical finding presents a significant problem for p-type GaN since not only is the associated point defect a compensating double donor, but the low growth temperatures needed for p-type GaN growth are also conducive to high incorporations of these defects. These factors will be revisited in the results of this work.

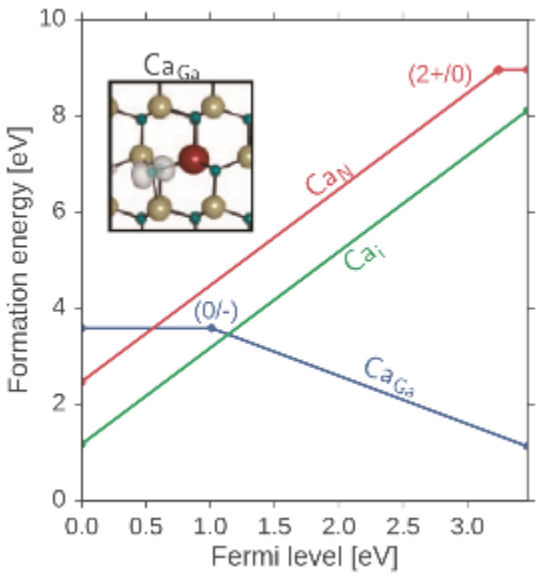


Figure 15: Formation energy of various Ca point defects in GaN with respect to the system Fermi level[42].

Experiment

In order to study the effect of Ca on the *p-n* junction properties, two samples are grown – one with and one without Ca reduction superlattice (ref. Chapter 2. Growth). The grown structures are given in **Figure 16**.

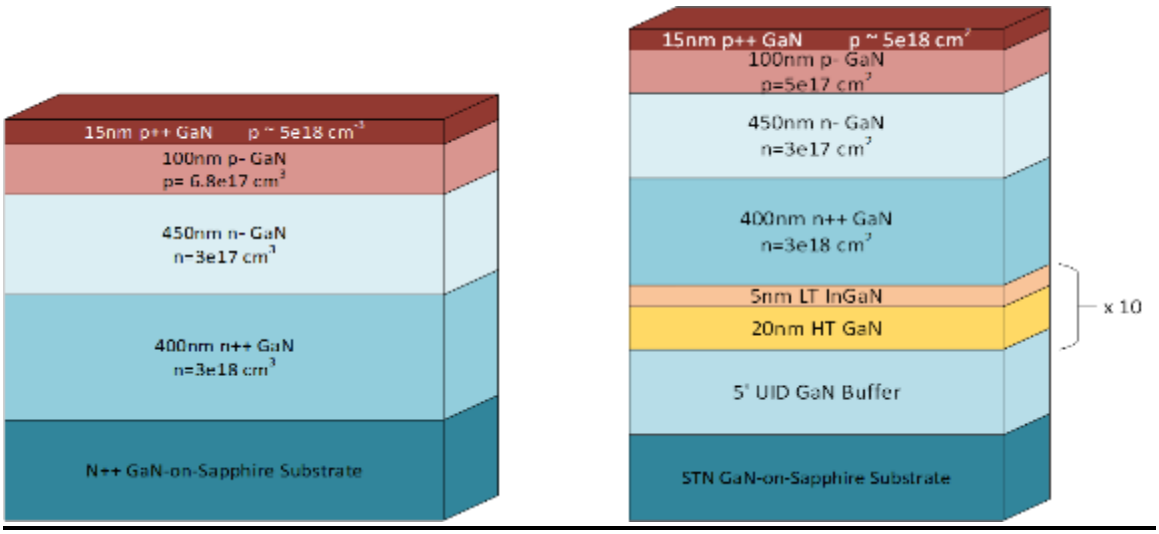


Figure 16: The structures grown in the work thus far by NH_3-MBE. a) A standard *p-n* junction grown with no pre-growth structures. b) A *p-n* junction diode grown with Ca reduction superlattices as a pre-growth treatment.

After the growth was completed, the samples were unloaded and then their morphologies were analyzed using AFM. Good surface morphology is dictated by the presence of spiral steps on hexagonal islands to confirm step flow was achieved during growth. RMS roughness should not exceed 5 nm over a 5 × 5μm or 1 × 1 μm area. Surface morphologies are shown in Figure 17. The presence of pits, while not noted at the time, was an indicator of an issue regarding the stability of the backside Ti metal in the NH_3-MBE environment (for more details, see Appendix D).

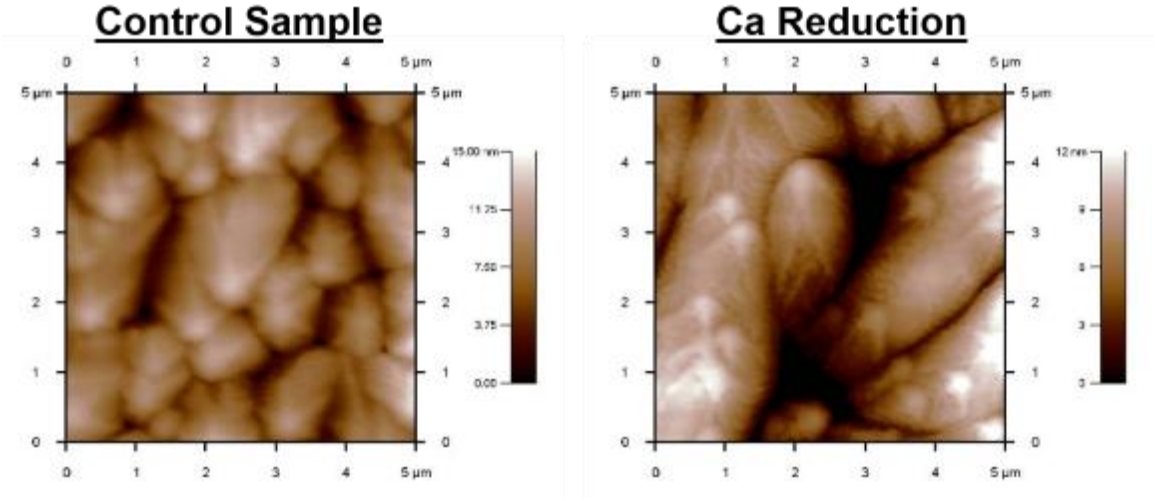


Figure 17: AFM scans were conducted after MBE growth.

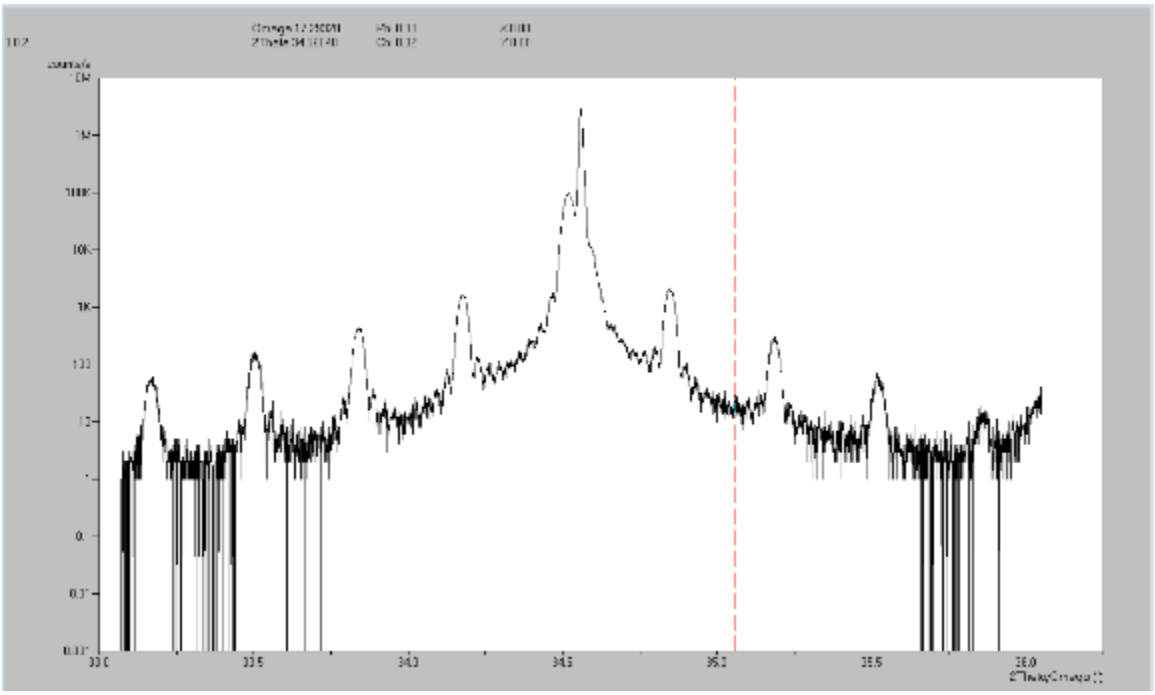


Figure 18: 3^{O} ω – 2θ scan to confirm the presence of a periodic superlattice beneath the GaN *p-n* junction diode.

After that morphology was measured by AFM, the Ca reduction sample was then scanned with a 3° ω – 2θ scan about the (002) reflection which revealed a periodic interference caused by the superlattice InGaN/GaN structure at the bottom of the device (Figure 18). Once the quality of the superlattice was confirmed, In dots are soldered onto the surface and side of the sample to form rudimentary contacts to the *p-n* junction to confirm that the sample showed a rectifying junction and a current turn-on at ~3 V forward bias. At this point, the samples have demonstrated satisfactory morphological, crystallographic, and electrical characteristics, thus they were transferred to the cleanroom to undergo Passivation processing (ref. 0. Chapter 3. Processing).

After fabrication, the electrical data is measured with the DC Station and 4155B Parameter Analyzer in the High Frequency Measurements lab. Using needle probes, I-V curves for diode contact pads of different sizes are obtained. A -5V to 5V DC sweep with a 100mA compliance

was the standard low-voltage measurement that was done to observe leakage and on-state characteristics. After the devices were measured, the cTLMs are then current swept using a 4-probe Kelvin measurement. The n-contacts were current swept from -10 mA to 10 mA with a 2 V compliance while the p-contacts are current swept from -1 mA to 1 mA with a 5 V compliance due to higher expected Ohmic resistances. Current density-voltage (J-V) plots are shown in **Figure 19** and **Figure 20**– note that **Figure 20** is plotted in a ln(J) scale for the purposes of calculating ideality.

Analysis

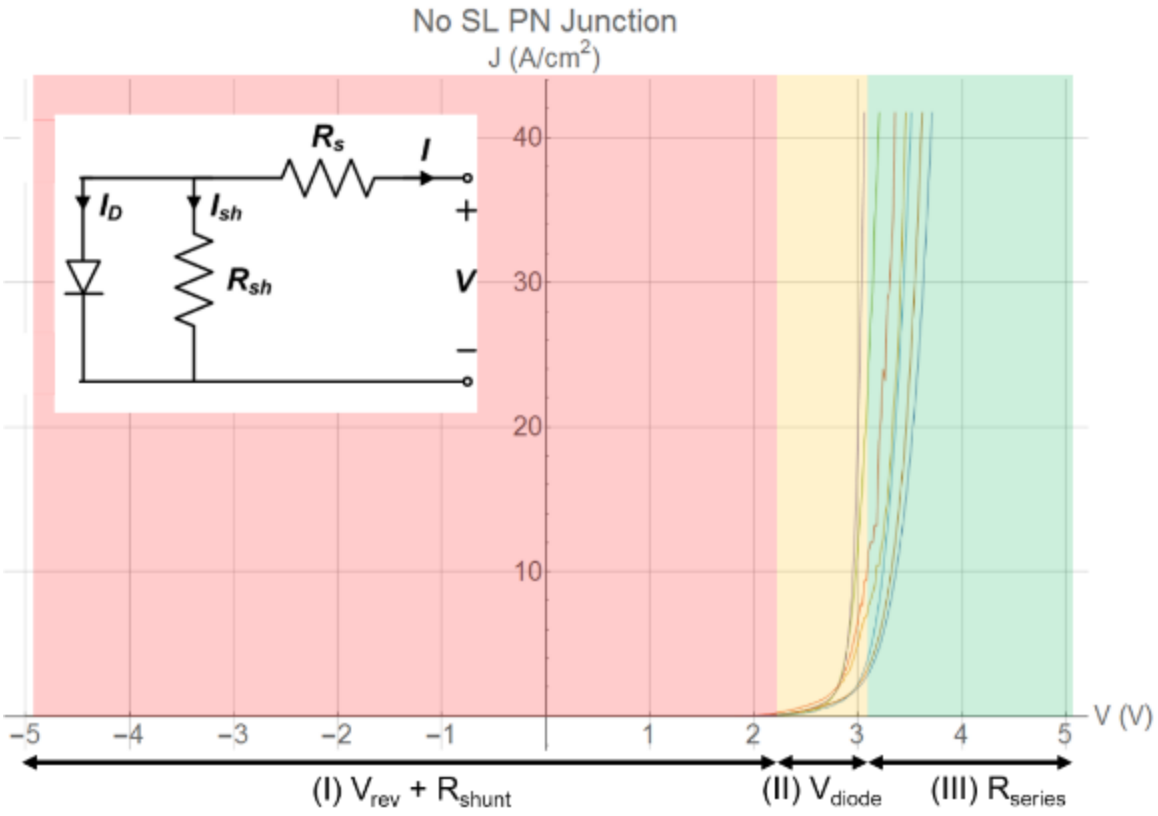


Figure 19: Under the Single Diode Model (SDM), there are three main components of the equivalent circuit (inlay) that are easily seen in the data. (I) The V_{rev} and R_{shunt} regime is current limited by the parallel resistance of the reverse bias diode and any parasitic current pathways. (II) The V_{diode} regime is characterized by the rapid change in dynamic resistance of the diode as the ideal diode goes from a high to low resistance component. This action effectively

short circuits the shunt impedance making it an essential open in the circuit. (III) The R_{series} regime is choked by the series resistance (contacts, measurement tools, etc.) as the diode becomes a near zero impedance component in the circuit.

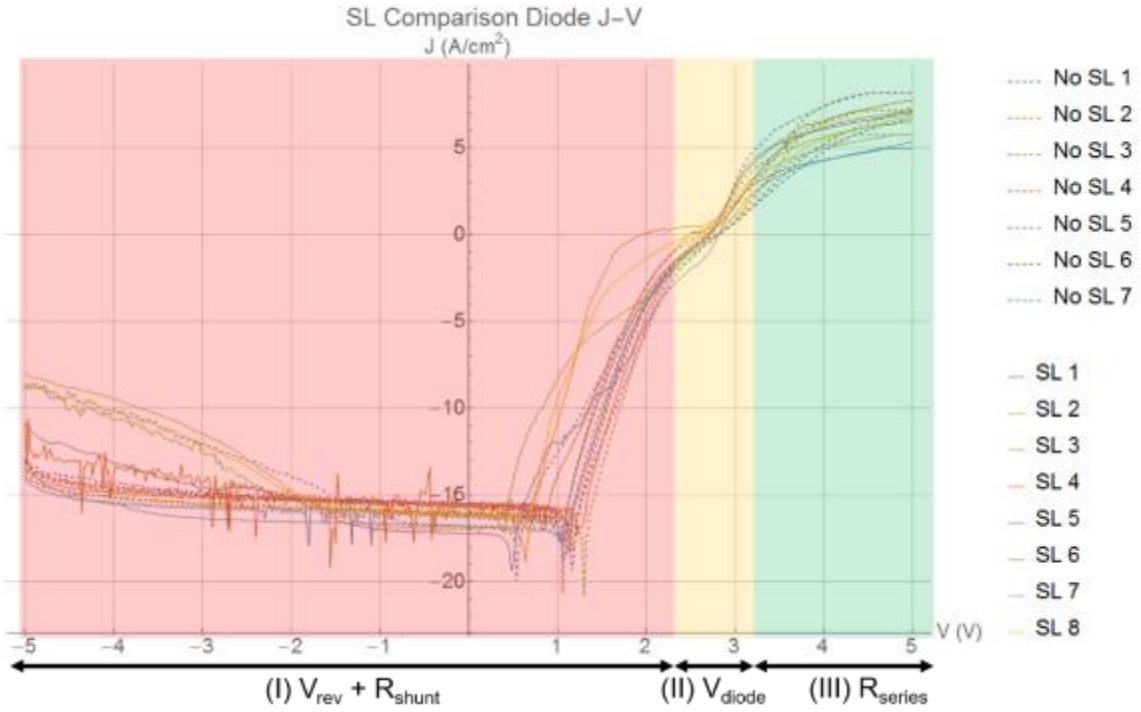


Figure 20: When plotted on a log scale, the parasitic currents, leakages, and turn-on voltages become clearer. Labels for the different passive component regimes are included from **Figure 19**. Note that these measurements were taken while the device was illuminated thereby resulting a noticeable offset at low voltages.

As raw I-V is not particularly useful for materials analysis, the first step in analysis is to derive the current density normalized over the area of the contact. To assess the quality of the diodes, the resistances of the passive components of the whole fabricated diode are derived – an equivalent circuit diagram of the Single Diode Model (SDM) used for this study is shown in Figure 19. From the linear J-V plots, the normalized contact resistance can be derived from the linear regions of the J-V curves. The results of these calculations as well as the cTLM analyses are shown in Table 5. The curves are then plotted on a natural log scale (Figure 20) to gain a clearer picture of its different regimes as in Figure 19. After passive resistances and

general material properties are derived, the ideality of the diode is then calculated using the ln(J)-V curve and the ideal diode equation:

$$J = J_0 e^{\frac{qV}{nkT}} \quad (5)$$

$$\ln(J) = \ln(J_0) + \frac{q}{nkT}V \quad (6)$$

In these equations, J is the current density, J_0 is the reverse bias saturation current, q is the electron charge, V is the applied voltage, n is the ideality factor, k is Boltzmann's constant, and T is temperature. This analysis is done as a point-to-point linear regression analysis with a 10-point spread. This analysis yields an ideality curve as shown in **Figure 21**.

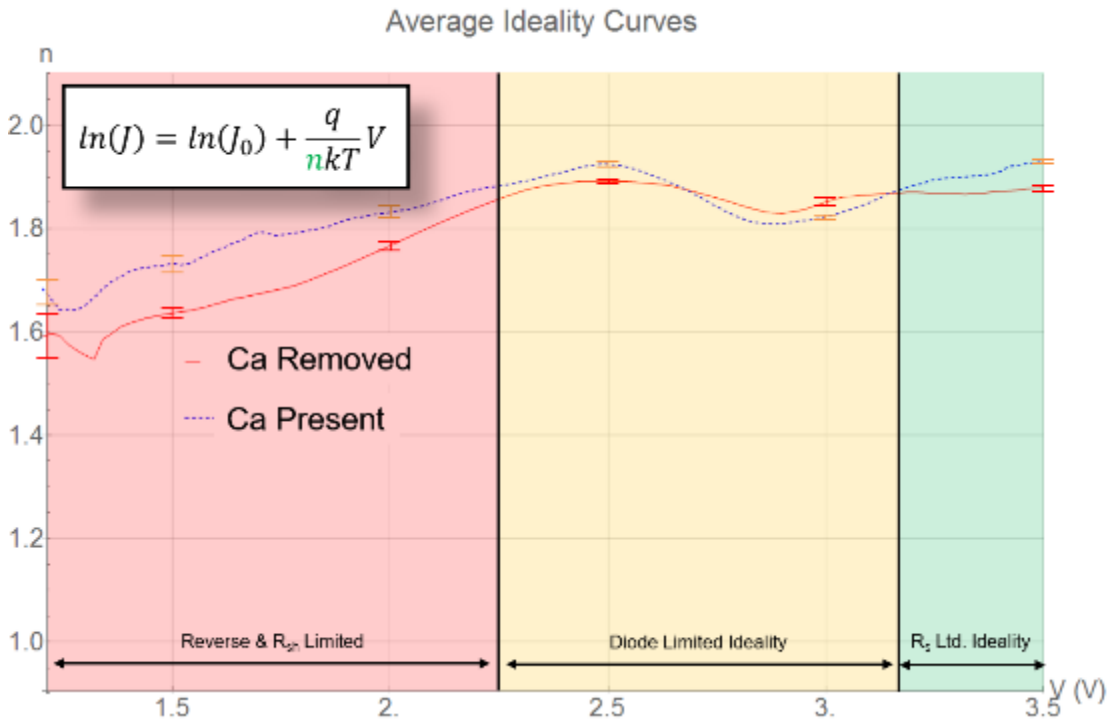


Figure 21: Diode ideality comparison plots with previously described diode regimes.

	Standard Growth		Ca Reduction Growth	
	n-Contact	**p-Contact**	**n-Contact**	**p-Contact**
R_{series} (Ω cm^2)	4.7×10^{-3}		1.2×10^{-2}	
R_{shunt} (Ω cm^2)	2.8×10^{6}		2.2×10^{6}	
R_{sh} (kΩ / $\square$)	2.4	160	4.8	75
ρ (Ω cm)	4.7×10^{-2}	1.8	9.6×10^{-2}	0.87
L_T (μm)	0.32	0.33	0.24	1.03
ρ_C (Ω cm^2)	3.8×10^{-4}	2.6×10^{-2}	5.9×10^{-4}	4.0×10^{-2}

Table 5: Results from J-V and cTLM measurements.

Discussion

The electrical differences between the standard and superlattice samples reveal interesting insights into the behavior of Ca in the functional components of a *p-n* junction diode. In the junctions grown for this work, the n-type side was lightly doped to make an asymmetric diode; this asymmetry results in the depletion region being confined to the n-type side of the junction. As has been noted, n-type GaN grows at a much higher temperature thus has a much lower incorporation rate for Ca (0.03% of the surface concentration incorporation per monolayer of growth. This indicates that the incorporation of Ca in the high temperature, n-type region in which the depletion region exists is likely too low to have any significant effect on the transport characteristics of the device relative to the other defects that are present in the film like threading dislocations.

Although there was not a significant difference in the ideality factors of the diodes in this study, the dramatic difference in device series resistances shown in Table 5 (4.7×10^{-3} vs. 1.2×10^{-2} Ω cm^2) stands out most prominently; this in conjunction with the notable difference in

specific p-contact resistances (2.6 x 10^{-2} vs. 4.0 x 10^{-2} Ω cm^2) seems to indicate the p-contact interface resistance is the predominant cause of this difference.

It has been calculated that Ca forms a deep acceptor Ca_{Ga} state 1.01eV above the valence band edge in n-GaN and a shallow double donor Ca_i when the Fermi level is < 1.25eV above the valence band edge[42]. This may indicate that the Ca that rides the growth surface and gets incorporated into the crystal may assist in carrier conduction through the metal-semiconductor interfaces. With this defect state at the interface, thermionic-field emission through the Schottky interface could be mediated; without this defect state, the emission through the barrier would be substantially less and force the electric field to overcome the Schottky barrier.

Additionally, there is a substantial difference in the bulk resistivity and sheet resistance of the p-GaN regions of the two samples measured using patterned cTLMs. This reduction in resistivity could be attributable to two phenomena as can be seen by observing the resistivity equation

$$\rho_p = \left[q\left(\cancel{\mu_n n} + \mu_p p\right)\right]^{-1} \approx \left[q\mu_p p\right]^{-1} \tag{7}$$

where ρ_p is the resistivity of the p-GaN, q is the electron charge, μ_n is the electron mobility, n is the electron concentration, μ_p is the hole mobility, and p is the hole concentration. Since we are observing the properties of p-type material, the electron-term of the equation can be ignored since $n \ll p$ as shown in Equation (7). This means that the Δρ observed between the Ca reduction sample and the control can be due to either a 52% decrease in the hole concentration due to Ca capture, a 52% decrease in the mobility due to increased scattering from the ionized acceptors and double donors, or a combination of both. Experimental verification of Ca effects on mobility would require the growth of Hall samples specifically to observe this effect and

were not conducted in the course of this research due to conflicting research projects. Preliminarily verifying an effect of hole reduction due to Ca can be much more easily accomplished on the samples that were measured by conducting SIMS measurements. From Equation (7), it can be quickly calculated that a 52% decrease in the resistivity can be attributed to the removal of $4 \times 10^{17}\ cm^{-3}$ hole concentration due to the shallow Ca_i double donors correlating to a concentration of $[Ca] = 2 \times 10^{17}\ cm^{-3}$. This value is very closely in line with the expected concentration of Ca given an initial surface dose of $\theta = 1.3 \times 10^{12}\ cm^{-2}$ with an segregation rate, $R = 98.4\%$[40]. These values are in line with our previous work into the incorporation rates of Ca in MBE grown GaN material[40] and were verified by SIMS measurements of the p-GaN material showing $[Ca] = 1.87 \times 10^{17}\ cm^{-3}$. Although this result shows a non-negligible incorporation of Ca into GaN during p-type growth conditions and its measurable effect on the electrical properties of the grown p-GaN material, this result does not definitively conclude whether Ca_i increase material resistivity by primarily reducing carrier concentration or increasing ionized impurity scattering. This will be further discussed in Chapter 6.

Threading Dislocation Density

Introduction

III-N semiconductors have been widely used in high-speed transistors[1–5], visible and ultraviolet (UV) optoelectronics[6–12], and vertical power electronics[13–17]. The high theoretical breakdown field (~3.3 MV/cm) and drift carrier mobilities (>1,000 cm^2/V-s) have garnered interest in the field of power electronics where energy efficiency and high voltage operation are necessary. Vertical device topologies are useful for reducing the wafer footprint of power electronics by allowing voltage to be held across epitaxially grown interfaces rather than lateral

ones. One of the major challenges to the performance of GaN vertical power devices has been the ubiquitous presence of threading dislocations (TDs) in the substrates for epitaxial growth. TDs have been repeatedly shown to exacerbate catastrophic and non-catastrophic breakdown in vertical GaN devices[16,35,43], but the mechanisms by which this occurs has been hitherto unstudied despite being experimentally observed.

The dislocation structure in GaN has been extensively studied by high-resolution x-ray diffraction (HRXRD) and transmission electron microscopy (TEM). Edge and mixed-type threading dislocations have been shown to be much more prevalent than their screw-type counterparts, but they all have a line vector within ~10° of the <0001> direction regardless of their Burgers vector, $\vec{\boldsymbol{b}}$ [25,26]. Furthermore, the electrical nature of TD trap states in n-GaN has been shown to be a deep acceptor in the band gap with a line density of approximately one electron trap state per c-lattice translation. It has also been observed that this trap state density associated with TDs results in a screening region around the dislocation as the donors interact with the trap states to create regions of significant net charge. In a simple picture, the occupied dislocation-related acceptors in n-type material are screened by ionized donors as shown in Figure 29. Similarly, we assume that dislocation-related donors are screened by ionized acceptors in p-type material.

The ionization and screening of the cylindrical area of the TD line distorts the energy band profiles around the dislocation with potentials of ~2.5 V as observed by electron holography in n-GaN[28]. This behavior has been attributed to the coalescence of defects around the TD core as suggested by Arslan and Browning[32] and observed by Müller et al.[29]. The trap state energy associated with such a band bending closely matches an electron trap state ~1.0 eV above the valence band maximum found in DLTS measurements[44]; additionally, the trap state density

are consistent with previous experimental and theoretical values of approximately one electron trap state per c-lattice translation[45]. From these experimental observations and theoretical predictions, it is possible to construct an accurate band structure model of n-type GaN pierced by a TD.

In our previous work, we derived a model to explain experimentally observed leakage by which these dislocation distortions of the surrounding band structure resulted in a reduced diffusion barrier for leakage in forward bias. This reduction in the diffusion barrier allows electrons and holes to occupy the junction near the dislocation thereby causing a spike in the np-product that results in a high Shockley-Read-Hall recombination disk that further exacerbated forward bias leakage. In this work, we compare our experimental diodes to our modeling to confirm the physical accuracy of the previous results.

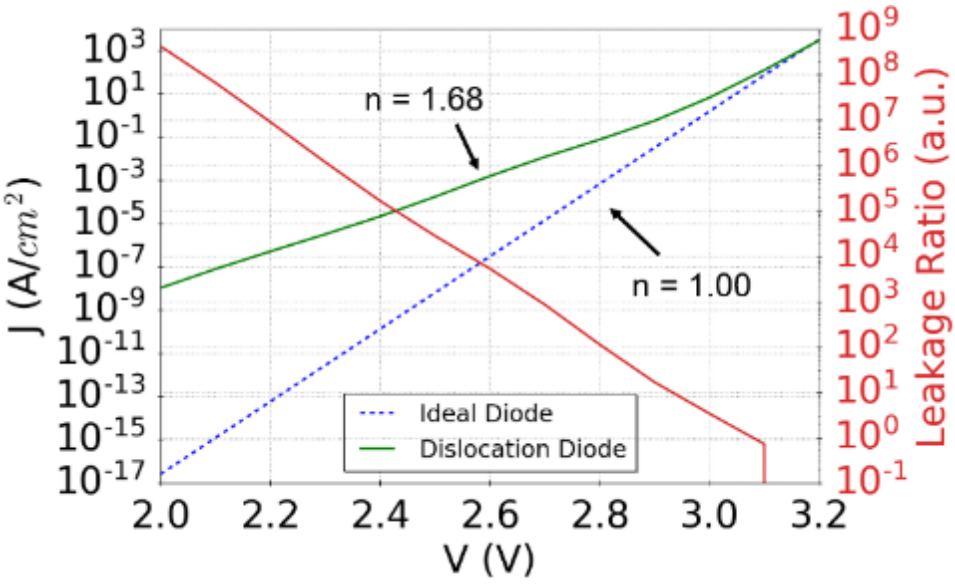


Figure 22: J-V curve given in Chapter 5 of this work comparing dislocated diode leakage to an ideal GaN diode.

Experiment

In this study, samples were grown in a Veeco Gen 930 molecular beam epitaxy system. The system has conventional effusion cells for Ga, In, and Si. Mg doping was controlled by a

valved source to provide consistent Mg concentrations compared with standard effusion cells in NH_3-MBE systems. Purified NH_3 was delivered into the growth chamber via an unheated showerhead injector. Temperature was measured in situ using a 1.6 μm pyrometer to measure a backside metal stack of Ti/Pd/Ti deposited by electron beam evaporation to ensure temperature accuracy in the high temperature, NH_3 environment. Sample A was grown on GaN-on-sapphire with a threading dislocation density (TDD) ~ $3 \times 10^8\ cm^{-2}$, and Sample B was grown on free-standing (FS) GaN with a $TDD \sim 2 \times 10^6\ cm^{-2}$. Both GaN substrates are heavily doped with Si. A schematic of the growth structure is shown in Figure 23.

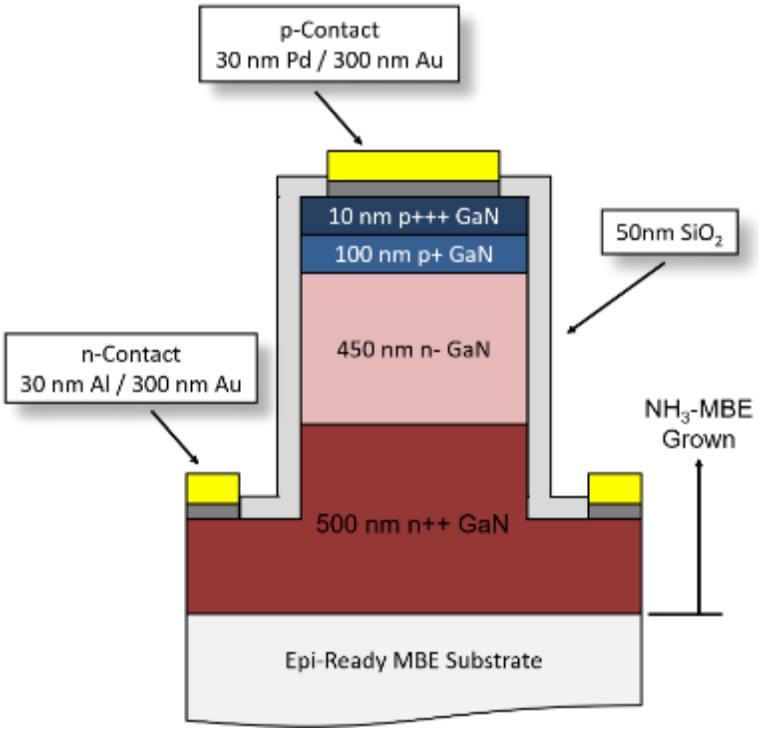


Figure 23: Schematic diagram of NH_3-MBE grown vertical *p-n* diode. The lightly doped, n- region thickness is calculated based on the depletion region width at the approximate breakdown voltage of the device as predicted by Sze and Gibbons[41] and used by Baliga[19].

Before growth, an *ex situ* solvent cleaning procedure was done by sequentially immersing the samples in acetone, methanol, and isopropanol in a high power ultra-sonic bath to remove any surface contaminants. Each substrate was then loaded into a molybdenum block

using faceplates and pyrolytic BN (PBN) rings to provide thermally stable tension necessary to hold the sample in place. Once loaded into the blocks, the samples were backed at $150\ °C$ for 1.5 hours to evaporate water from the samples. The samples were then transferred into a buffer chamber where they were individually baked at $400\ °C$ for 1 hour to further degas the block. After baking, the sample block is then transferred into the growth chamber for epitaxial growth. When the substrate temperature exceeded $450\ °C$, 200 sccm of NH_3 is flowed to prevent GaN decomposition during the chamber preparation. This flow rate is maintained through growth.

A 500 nm, heavily doped GaN:Si layer was grown at a substrate temperature of $820\ °C$ under a Ga beam equivalent pressure (BEP) of $2.7 \times 10^{-7}\ torr$. A 450 nm, lighly doped GaN:Si was then grown by maintaining the same Ga BEP and NH3 flow while lowering the Si effusion temperature from $1450\ °C$ to $1250\ °C$. This process takes 5 minutes to run and was performed without a growth interrupt to avoid any surface contamination at the interface. These growth conditions were calibrated to a growth rate (GR) of 500 nm/hr with step-flow growth confirmed by atomic force microscopy (AFM). At the metallurgical interface, a 5' growth interrupt occurs to allow for the shift in substrate temperature for n- and p-type GaN.

A 100 nm GaN:Mg layer was then grown at a substrate temperature of $750\ °C$ under a Ga BEP of $1.2 \times 10^{-7}\ torr$ and an In BEP of $5 \times 10^{-8}\ torr$. The In is included during all p-GaN growths for this study to minimize the generation of surface defects due to high Mg doping in GaN[37]. Additionally, the growth conditions were optimized to maximize the p-GaN conductivity while sustaining a smooth surface morphology with low pit density. To avoid Mg contamination of the n-GaN, our valved source was kept close until this p-GaN layer growth is initiated at which point it is opened to 50% of maximum opening. Finally, a 10 nm, very

heavily doped GaN:Mg layer was grown by increasing the Mg valve opening from 50% to 75%. Table 6 provides a summary of the individual layer properties and the calibration techniques used.

	Calc.	**HR XRD**	**SIMS**		**Hall Effect**	
	t (nm)	GR (nm/hr)	$N_D\ (cm^{-3})$	$n\ (cm^{-3})$	$\mu_n\ \left(\frac{cm^2}{Vs}\right)$	$\rho\ (\Omega - cm)$
n++	500	500	1×10^{20}	9.7×10^{19}	116	5.7×10^{-4}
n-	450	500	5×10^{17}	3.1×10^{17}	437	4.5×10^{-2}

	t (nm)	**GR (nm/hr)**	$N_A\ (cm^{-3})$	$p\ (cm^{-3})$	$\mu_p\ \left(\frac{cm^2}{Vs}\right)$	$\rho\ (\Omega - cm)$
p+	100	200	1×10^{20}	2.2×10^{18}	4.5	0.66
p+++	10	200	3×10^{20}	---	---	---

Table 6: Summary of individual layer properties in grown structures.

After growth, the surface morphologies were characterized by AFM to confirm that growth occurred in the quasi-stable growth condition[39] where the high quality GaN growth in N-rich NH_3-MBE occurs. The micrographs are given in Figure 24.

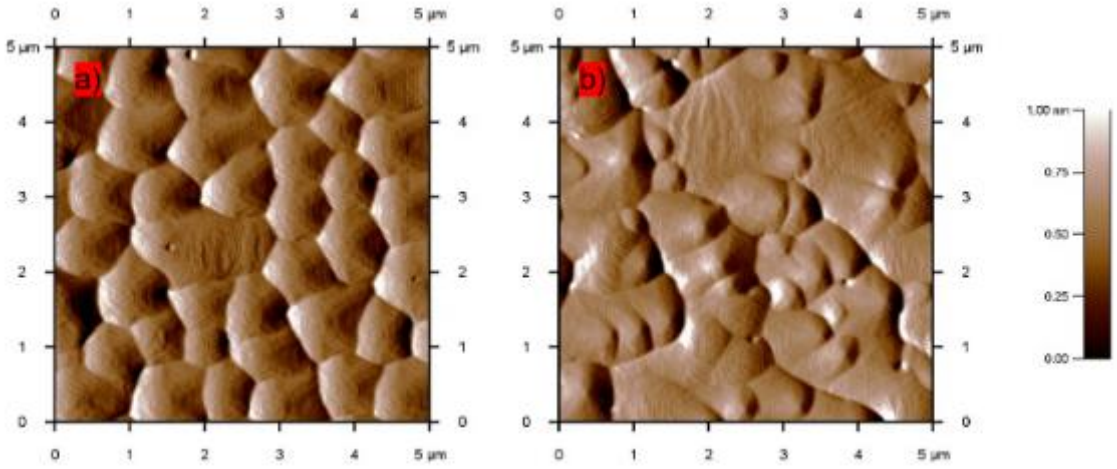


Figure 24: AFM micrographs for the a) STN and b) FS GaN p-n diode growths.

After good surface morphology was confirmed with AFM, the samples were simultaneously processed using the flow shown in Figure 25. The samples were first thorough solvent cleaned in acetone, methanol, and isopropanol with high powered ultra-sonication to removal any surface contaminants that reside on the surface with exposure to dirty atmosphere., The samples were then soaked in hydrochloric acid (HCl) for 5' and then Buffered HF (BHF) for 10' to remove metallic contaminants and surface oxides, respectively. The samples are then immediately transferred from BHF into a plasma-enhanced chemical vapor deposition (PECVD) chamber where a 50 nm layer of SiO_2 was deposited. This thin layer of oxide is used to protect the p-GaN surface to assure good p-contact properties; the layer thickness is optimized to allow for adequate surface protection from subsequent processes while also being thin enough to be reliably removed in its entirety in a 60" BHF dip that does not damage photolithographic patterning.

After the SiO_2 deposition, the sample were then patterned using photolithography to expose select areas of the protecting oxide. This protecting oxide was then etched with a 60" BHF dip to expose the regions of the device designated for mesa etching. The sample was then transferred into a reactive ion etch (RIE) chamber where it underwent a 100 W Cl_2 etch (etch rate ~75 nm/hr) to isolate the diode mesas as well as the p-contact cTLM mesa. The sample was removed the chamber and immediately submerged in DI water to remove any Cl contamination on the surface of the damaged GaN sidewalls. The photoresist and SiO_2 were then stripped from the sample using AZ NMP Rinse and BHF sequentially; the samples are then immediately transferred back into the PECVD chamber where another conformal layer of 50 nm of SiO_2 was deposited onto the surface. This deposition continues to protect the p-contact interface but now also passivates the sidewalls with an insulating oxide layer to

mitigate sidewall leakage effects. Circular p-contacts of differing radii consisting of 30 nm Pd / 300 nm Au were deposited using an electron beam evaporation system and liftoff photolithography. Finally, a blanket n-contact consisting of 30 nm Al / 300 nm Au was similarly deposited using electron beam evaporation and liftoff photolithography.

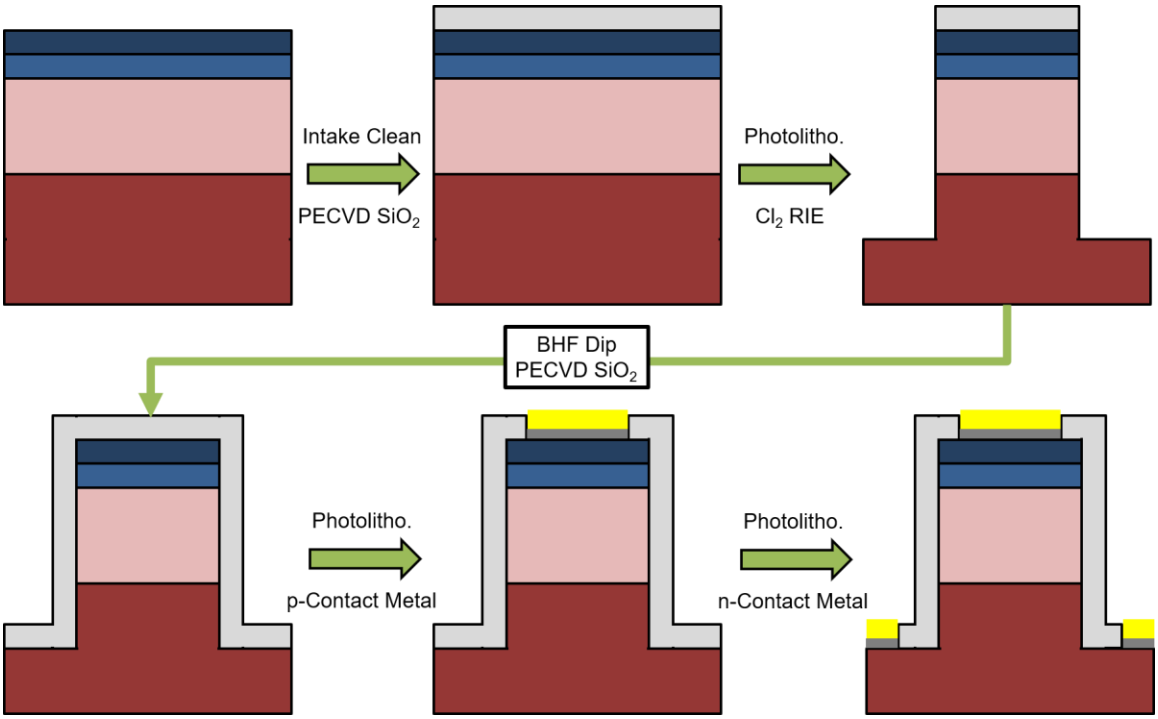


Figure 25: A schematic diagram of the fabrication processed used for the p-n diodes in this work.

The fabricated samples were then electrically measured using a 4155B and DC probe station. The first measurement confirms linear behavior of the contacts by measuring cTLM on the p- and n-type GaN using a 10 mA current sweep with a 10 V compliance limit. The cTLMs have a radius of 50 μm and ring spacings of 15, 12, 10, 8, 6, 5 μm. The contact properties are given in the Results section.

Once contact integrity is confirmed, the diodes are then measured using a 5 V DC voltage sweep with a 100 mA compliance limit. Since leakage and low-current characteristics are being measured, steps were taken to mitigate extrinsic leakage mechanisms. Before

measurement, probes were tested for leakage paths using an automated, internal system and using standard open probe measurements to ensure leakage currents were less than 1 pA. To mitigate leakage due to contact with the metal measurement stage, a glass slide was also placed underneath the sample to isolate it from the system. Lastly, measurements were taken in the dark in order to mitigate photogenerated current in these electrical measurements.

Prior to measuring the diodes, the contact properties were measured via a current sweep on cTLM structures on both the n- and p-type GaN. The contact I-Vs (Figure 26) and properties (**Table 7**) are given below. Note that the I-Vs for the p-contacts see an increase at ~3.1 V due to the diode beneath the measured p-layer.

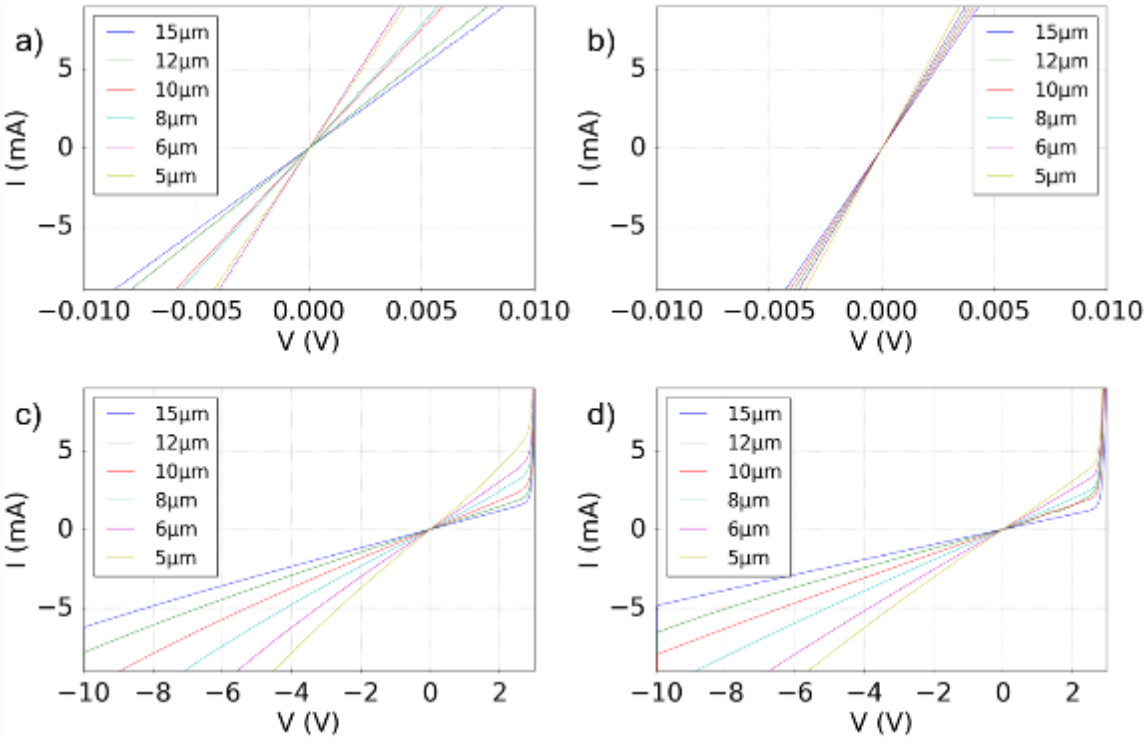


Figure 26: cTLM curves for a) n-contacts on n^{++} GaN-on-Al_2O_3, b) n-contacts on FS, c) p-contacts on STN, and d) p-contacts on FS. Note that in b) and d), the I-V curves rise sharply when the potential across the cTLM ring exceeds 3 V. This behavior is due to the floating bias of the n-side of the *p-n* junction beneath the cTLM; when the voltage in the p-GaN region of the device exceeds the built-in potential of the junction, carriers can flow through the diode and the n-type regions of the device.

	GaN-on-Sapphire		FS GaN	
	n-Contact	p-Contact	n-Contact	p-Contact
$\boldsymbol{\rho_C\ (\Omega - cm^2)}$	5.0×10^{-6}	8.3×10^{-4}	1.4×10^{-5}	1.0×10^{-3}
$\boldsymbol{\rho\ (\Omega - cm)}$	---	0.36	---	0.44
$\boldsymbol{R_{SH}\ (\Omega/\square)}$	20.6	3.6×10^{4}	4.1	4.4×10^{4}
$\boldsymbol{L_T\ (cm)}$	9.6×10^{-5}	9.3×10^{-6}	1.3×10^{-3}	9.3×10^{-6}

Table 7: Extracted contact and material properties from cTLM measurements.

With the contact properties confirmed, the diode electrical characters were measured and are shown in Figure 27. As has been previously reported by other growth methods, these diodes grown by NH_3-MBE exhibit a diminishing effect from leakage due to dislocations as the diode turns on due to the screening of the dislocation-associated effects and leakage.

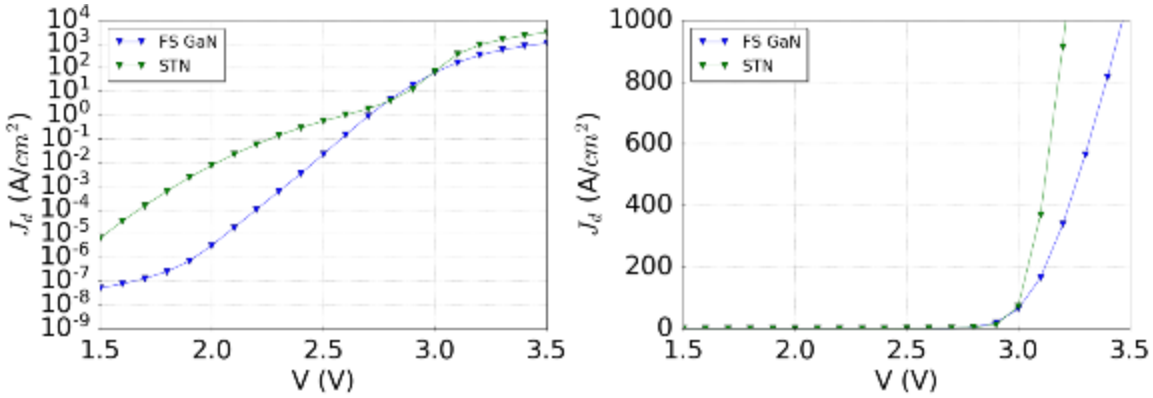


Figure 27: Experimental current density vs. voltage curves for the two diodes in this study.

As has been previously reported by MOCVD and PAMBE, we observe a significant correlation between TDD and leakage current in GaN *p-n* diodes. A comparison of the experimental diodes to the models presented in our previous work is given in Figure 27. In Figure 27b), the rectification occurs at ~3.0 V with the high TDD sample having a lower series resistance due to the previously observed lower contact resistivities associated with the higher TDD sample. Furthermore, it can be observed in Figure 27a) that as the diode approaches turn-on (~2.8 V), the different TDD samples' J-V curves converge on the same behavior consistent with prior experimental and theoretical work in other growth methods.

Models of the fabricated diode were then ran using a Gaussian distribution of trap states and variable r-mesh limits to approximate the observed TDD in the sample. Experimental contact resistivities were also added to ensure the model appropriately considered the regime of the J-V dominated by the series resistance. Although the models do not have numerical accuracy with regards to the experimental diodes, their behavior is quite similar with respect to the convergence behavior as the dislocation and depletion fields collapse. This discrepancy could be due to many factors on the experimental diodes that are not considered in the model such as sidewall associated leakage due to small device size (≤ 50 μm) or other impurities present in both structures that causes higher current leakage at low voltage in both devices while still allowing TDD effects to be seen.

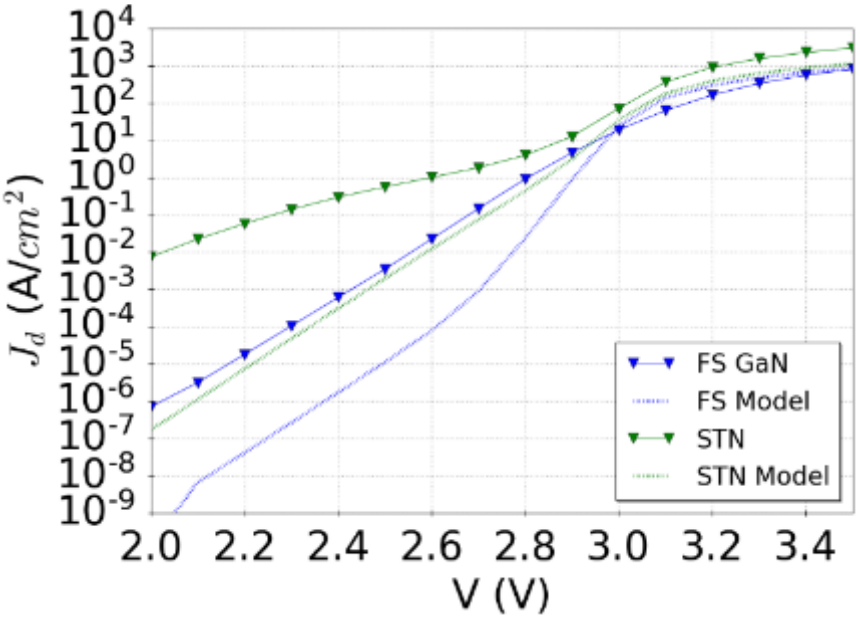


Figure 28: Measured J-V curves compared to results given by the model discussed in Chapter 5. Note that the x-axis of this plot begins at 2 V due to the noise floor of the models used for this comparison.

This is likely due to a fundamental limitation of the cylindrical symmetry used for creating these 2D models. Since the symmetry can only approximate a single dislocation with a region of perfect crystal around it, it is unable to model the effects of interactions between different

threading dislocations on leakage. Furthermore, in simulations with a mesh radius of less than 60 μm, the model does not converge on a current profile observed in a diode model with no dislocation; this indicates that there are still effects of the dislocation beyond the boundaries of the problem. This indicates that if we had these dislocation densities, they would not only leak by their own interactions with the junction but only through interactions with other dislocations. This result presents an interesting prospect for future work in modeling and understanding dislocation related leakage mechanisms in GaN *p-n* junctions.

Summary & Future Work

In this work, two GaN *p-n* diodes are grown by NH_3-MBE on two 1 cm × 1 cm substrates with different threading dislocation density (TDD). The samples were then processed to fabricate mesa-isolated devices with varying radii as well as circular transmission line measurement (cTLM) structures for contact and material characterization. Low-resistance ohmic contacts were confirmed for both the n- and p-type contacts of the device. The diodes were then measured in the dark using a 4155B Parameter Analyzer and a DC probe station to measure the leakage behavior of the diodes. Rectification and TDD-dependent leakage were both observed and compared to previous work modeling dislocation-related leakage currents discussed in 0. Chapter 5. Defect-Mediated Leakage . Although experimental leakage currents are not accurately modeled by our current modeling of leakage currents, the result provides insight into the potential future work on this topic as it relates to understanding all the mechanisms that are at play in dislocation related leakage currents. Models analyzing the coupling effects of the dislocations with each other must be conducted to fully understand how TDD affects leakage current, and, in order to facilitate this problem, better 3D modeling

techniques need to be formulated to enable dislocations requiring a fine 3D mesh to be modeled in a large space requiring a rougher mesh.

Chapter 5. Defect-Mediated Leakage Modeling

Dislocation Mediated Forward Bias Leakage

Introduction

III-N semiconductors have been widely used in high-speed transistors[1–5], visible and ultraviolet (UV) optoelectronics[6–12], and vertical power electronics[13–17]. The high theoretical breakdown field (~3.3 MV/cm) and carrier mobility (>1,000 cm^2/V-s) have garnered interest in the field of power electronics where energy efficiency and high voltage operation are necessary. Vertical device topologies are useful for reducing the wafer footprint of power electronics by allowing voltage to be held across epitaxially grown interfaces rather than lateral ones. One of the major challenges to the performance of GaN vertical power devices has been the ubiquitous presence of threading dislocations (TDs) in the substrates for epitaxial growth. TDs have been repeatedly shown to exacerbate catastrophic and non-catastrophic breakdown in vertical GaN devices[16,35,43], but the mechanisms by which this occurs has been hitherto unstudied despite being experimentally observed.

The dislocation structure in GaN has been extensively studied by high-resolution x-ray diffraction (HRXRD) and transmission electron microscopy (TEM). Edge and mixed-type threading dislocations have been shown to be much more prevalent than their screw-type counterparts, but they all have a line vector within ~10° of the <0001> direction regardless of their Burger's vector, $\vec{\boldsymbol{b}}$ [25,26]. Furthermore, the electrical nature of TD trap states in n-GaN has been shown to be a deep acceptor in the band gap with a line density of approximately one electron trap state per c-lattice translation. It has also been observed that this trap state density associated with TDs results in a screening region around the dislocation as the donors interact with the trap states to create regions of significant net charge. In a simple picture, the occupied

dislocation-related acceptors in n-type material are screened by ionized donors as shown in Figure 29. Similarly, we assume that dislocation-related donors are screened by ionized acceptors in p-type material.

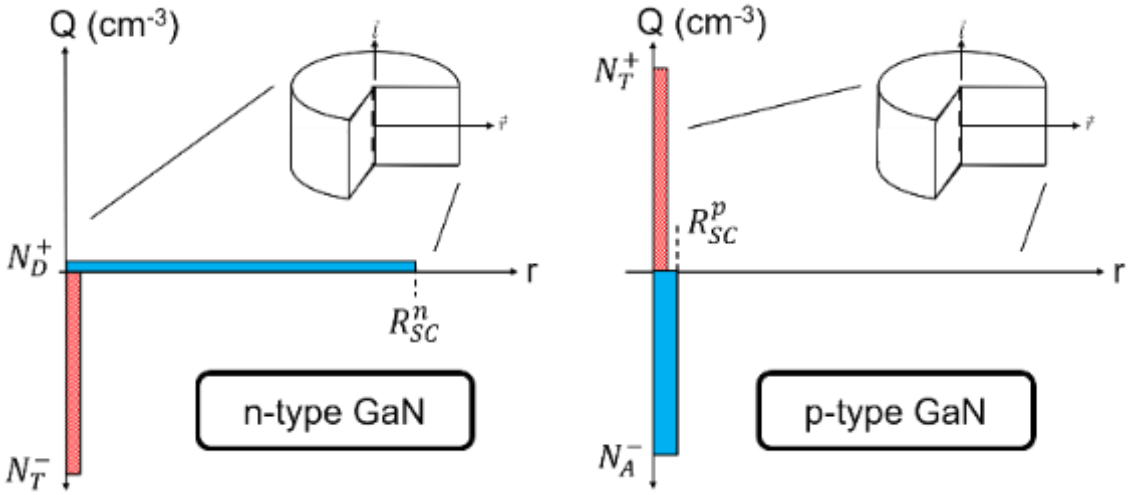


Figure 29: Simplified representation of screening regions around a dislocation in a lightly doped (N_D= 5×10^{17} cm^{-3}) n-type (left) and heavily doped (N_A= 5×10^{19} cm^{-3}) p-type (right) GaN. Note that the charge region around the dislocation in p-type GaN is much smaller than in n-type GaN due to the high doping required to produce p-type conductivity being on the order of the density of trap states.

In the simplest treatment, the dislocation and space charge regions are cylindrical with constant trap state and dopant density (Figure 29). The screening radius can be simply calculated using Charge Neutrality and results in

$$R_{SC} = \sqrt{\frac{\rho_n}{\pi c}} * \sqrt{\frac{1}{N}} \qquad (0)$$

where ρ_n is the number of trap states per c-lattice translation, c is the c-lattice constant, and N is the uniform dopant concentration of the semiconductor. This ionization and screening of the cylindrical area of the TD line distorts the energy band profiles around the dislocation with potentials of ~2.5 V as observed by electron holography in n-GaN[28]. This behavior has been

attributed to the coalescence of defects around the TD core as suggested by Arslan and Browning[32] and observed by Müller et al.[29]. The trap state energy associated with such a band bending closely matches an electron trap state ~1.0 eV above the valence band maximum found in DLTS measurements[44]; additionally, the trap state density are consistent with previous experimental and theoretical values of approximately one electron trap state per c-lattice translation[45]. From these experimental observations and theoretical predictions, it is possible to construct an accurate band structure model of n-type GaN pierced by a TD.

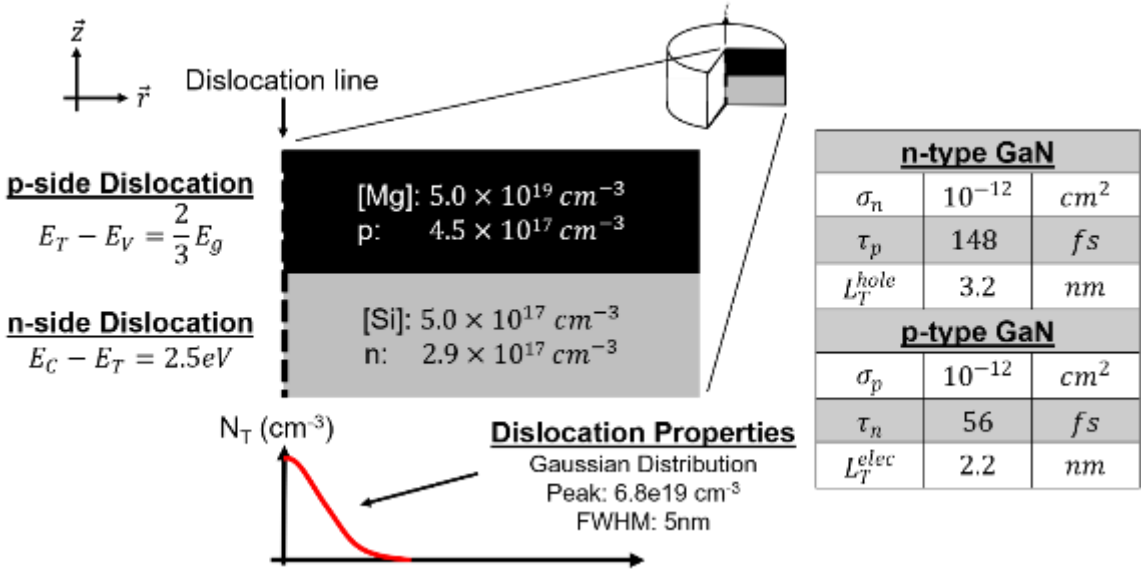
In contrast, a band structure model of p-type GaN that includes the treatment of TD trap states has been substantially more elusive. Electron holography analyses have found regions of negative space charge that is likely associated with screening acceptors around a donor trap states coalescing near TDs in p-GaN[28]. However, the high acceptor concentration needed to form achieve measurable hole conductivity results in a screening region that is beyond the resolution the holography method is likely able to measure accurately (~2 nm). Thus, the nature of the TD charge behavior in p-GaN remains experimentally unobserved. However, in our previous work, TDs in p-GaN act as nonradiative centers similar to n-GaN as shown by cathodoluminescence (CL) results[37], thus we assume that the TD trap states behave similarly in p- and n-type GaN.

These analyses indicate that in the unipolar bulk regions threading dislocations can be accurately described as a distribution of compensating trap states in the crystal along the TD line, but the interactions of the distortions in the band profiles of unipolar materials at a bipolar junction presents an interesting physical problem that has now been modeled. In this study, a physical model is presented to treat a vertical GaN *p-n* junction with a TD puncturing junction.

Energy band, electric field, and current flow diagrams are presented along with other plots of merit, and the mechanisms therein are discussed.

Model

In Appendix E, all relevant variables are given in alphabetical order to assist in understanding the parameters and models used in this work.



n-type GaN		
σ_n	10^{-12}	cm^2
τ_p	148	fs
L_T^{hole}	3.2	nm
p-type GaN		
σ_p	10^{-12}	cm^2
τ_n	56	fs
L_T^{elec}	2.2	nm

Figure 30. A cylindrically symmetric *p-n* diode is modeled for this study with a Gaussian distribution of deep trap states used to represent the TD-associated traps. Typical doping densities for the p- and n-type regions are used, and experimentally standard hole and electron concentrations are observed in the model. The location of the trap state energy within the n-type region was based on experimental results while the p-type region was placed arbitrarily deep in the energy gap. In the right table, values for trap capture cross section (σ), minority carrier lifetime (τ), and minority carrier diffusion length (L_T) are given for the trap state region associated with the TD line. These values were chosen such that these model variables all matched experimental values as closely as possible.

In this study, Silvaco's ATLAS modeling software was used to solve for the 2D *p-n* junction model shown in Figure 30. Cylindrical coordinates were used to simplify the computational requirements by utilizing the six-fold rotational symmetry of the 3D crystal

structure about the TD line vector, <0001>, without resorting to a full 3D treatment. N_A and N_D values are chosen based on experimentally typical values for vertical GaN *p-n* junctions doped with Mg and Si, respectively. The model r-dimension limit of 564 nm approximates a 10^8 cm^{-2} TD density as is typical in commercially available GaN growth on either Al_2O_3 or SiC. Our TD-associated trap state region was treated as a Gaussian distribution with FWHM of 5 nm and a peak trap state density of 6.84×10^{19} cm^{-3}. This distribution approximates a one electron per c-lattice translation when normalized in the z-direction. Trap energy levels within the bandgap were E_C – 2.5 eV and E_V + 2.3 eV for n- and p-type GaN, respectively. Although the energy level of the dislocation trap state in n-GaN is well-documented, the level for p-GaN is approximated as an arbitrarily deep donor state. This assumption will be discussed later.

The trap state properties are also chosen such that the minority carrier diffusion lengths and lifetimes match those given in the literature. Using the approximation of a $10^{16}\ cm^{-3}$ trap state density in the bulk away from the dislocation, a capture cross section for both electrons and holes of $10^{-12}\ cm^2$ was chosen based on the following equations:

$$\tau = (\rho_T * \sigma * \nu)^{-1} \tag{8}$$

$$L_T = \sqrt{\frac{kT}{q} * \mu * \tau}, \tag{9}$$

where τ is the minority carrier lifetime; ρ_T is the local trap concentration; σ is the trap minority carrier capture cross section; v is the minority carrier thermal velocity; L_T is the minority carrier diffusion length; and μ is the minority carrier mobility. These values resulted in a lifetimes and transfer lengths given in Table 8 using the minority carrier mobilities found by Kumakura et

al.[46]. The bulk values given in this table are within the expected range for minority carrier diffusion length and lifetime[46–49] and were observed in our diode model with no dislocation.

	$\rho_T\ (cm^{-3})$	τ_n	$L_T^n\ (nm)$	τ_p	$L_T^p\ (nm)$
TD core	6.84×10^{19}	56 fs	2.1	148 fs	3.2
Bulk	10^{16}	0.38 ns	178	1.01 ns	261

Table 8: Minority carrier lifetimes and diffusion lengths for different trap state conditions. The bulk lifetimes are within experimental parameters for minority carrier lifetimes[46].

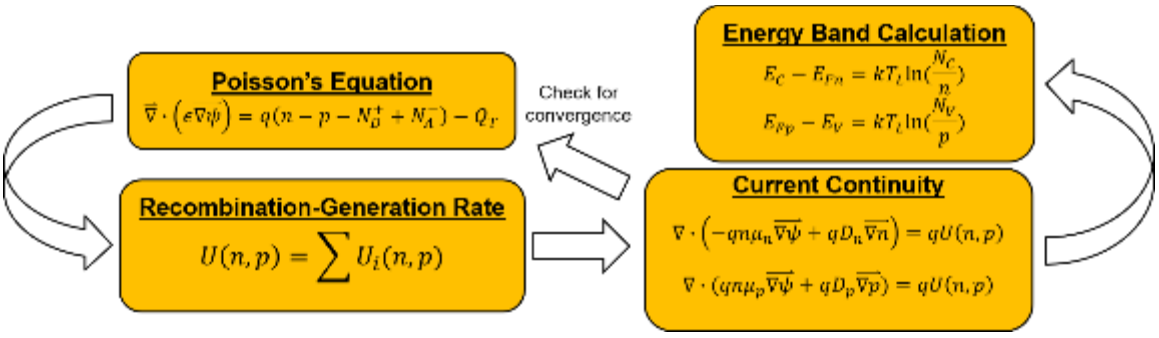


Figure 31. Process overview the Gummel method which was used extensively for modeling dislocation behavior; however, the Newton-Raphson methodology was used if convergence was not achieved.

Using this physical model, the Poisson and steady-state Current Continuity equations are solved on the mesh self-consistently using the Gummel method (Figure 31).

$$\vec{\nabla}\cdot\left(\epsilon\vec{\nabla}\psi\right) = q(n - p - N_D^+ + N_A^-) - Q_T \tag{10}$$

$$\nabla\cdot\overrightarrow{J_n} = -qU(n,p) \tag{11}$$

$$\nabla\cdot\overrightarrow{J_p} = qU(n,p) \tag{12}$$

In the Poisson equation (10), ψ is the electric potential; n and p are the electron and hole concentration; N_D^+ and N_A^- are the ionized donor and acceptor concentrations. In the Current

continuity equations, $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, and *U(n, p)* is the net recombination-generation rate. If convergence is not achieved, the solver will switch from the Gummel to the Newton-Raphson method to solve the system of equations.

In addition to these core equations, additional models are necessary to include the various behaviors of the GaN material systems and trap physics. These are discussed below.

Incomplete Ionization Model

It has been well-documented experimentally that Mg_{Ga} has an activation energy around 190 meV[50], thus to accurately model p-GaN, we utilized the incomplete ionization model[51] to account for the thermal activation of both the donors and acceptors in GaN.

$$N_D^+ = \frac{N_D}{1 + g_n exp\left(\frac{E_{Fn} - (E_C - E_D)}{kT}\right)} \tag{13}$$

$$N_A^- = \frac{N_A}{1 + g_p \exp\left(\frac{(E_A - E_V) - E_{Fp}}{kT}\right)}, \tag{14}$$

where N_D^+ and N_A^- are the ionized donor and acceptor concentrations; N_D and N_A are the donor and acceptor concentrations; g_n and g_p are the conduction and valence band degeneracies; E_{Fn} and E_{Fp} are the electron and hole quasi-Fermi levels; $(E_C - E_D)$ and $(E_A - E_V)$ are the donor and acceptor activation energies. This model predicts that only ~1% of the Mg acceptor dopants will contribute holes to the GaN semiconductor while ~60% of the Si donors will contribute electrons. Furthermore, unintentionally-doped GaN is usually slightly n- due to the unintentional doping by oxygen. This combined with the low activation efficiency necessitate high Mg concentrations to achieve p-type GaN experimentally.

Our model makes two basic doping assumptions. Firstly, the model uses an abrupt metallurgical junction such that there is no overlap between the p- and n-type regions of the

diode. Secondly, the model does not explicitly specify any compensating defects or recombination centers in the model away from the dislocation but rather combines the holistic crystal imperfections into a minority carrier lifetime within the range of values provided in the literature[46].

Shockley-Read-Hall (SRH) Trap-Assisted Recombination Model

To model the charging and screening effects around the dislocation line, a trap ionization model was implemented. The Simmons and Taylor model (based on Shockley-Read-Hall recombination statistics)[52–54] was used to simulate the occupancy, $f(E_T)$, and charge state density of trap states, Q_T, associated with the TD line:

$$Q_T = q(N_{tD}^{+} - N_{tA}^{-}) \tag{15}$$

$$N_{tA}^{-} = \rho_T * f(E_T) \tag{16}$$

$$N_{tD}^{+} = \rho_T * (1 - f(E_T)) \tag{17}$$

$$f(E_T) = \frac{\bar{n} + e_p}{e_n + \bar{n} + \bar{p} + e_p} \tag{18}$$

$$\bar{n} = \nu_n \sigma_n n \tag{19}$$

$$\bar{p} = \nu_p \sigma_p p \tag{20}$$

$$e_p = \nu_p \sigma_p N_V \exp(\frac{E_V - E_T}{kT}) \tag{21}$$

$$e_n = \nu_n \sigma_n N_C \exp(\frac{E_T - E_C}{kT}) \tag{22}$$

In this system of equations, Q_T is the concentration of charged trap states; N_{tD}^{+} and N_{tA}^{-} are the concentration of ionized donor and acceptor trap states; ρ_T is the density of trap states, $f(E_T)$ is the Fermi occupancy function at the trap state energy level; $\bar{n}$ and $\bar{p}$ are the electron and hole capture rates; ν_n and ν_p are the thermal velocities for electrons and holes; σ_n and σ_p

are the electron and hole capture cross sections; n and p are the electron and hole concentrations; e_p and e_n are the hole and electron trap emission rates; N_V and N_C are the effective density of states for the valence and conduction bands; E_V and E_C are the valence and conduction bands; and E_T is the trap state energy level. These equations tie into the previous models given in two important ways. Firstly, the electron and hole concentrations given in (19) and (20) are functions of the quasi-Fermi levels associated with the carriers. In forward bias, these quasi-Fermi levels split near the junction and would therefore change the behavior of the traps in these regions. This change carrier statistics in the regions with Fermi level splitting is considered in these two equations by the inclusion of the local carrier concentrations which are functions of the quasi-Fermi levels. Secondly, as previously stated, the trap states are given a capture cross section such that the minority carrier lifetimes and minority diffusion lengths in the bulk associated with a lower concentration of these traps matches with previously found experimental evidence. The chosen values for capture cross section also come into effect here when calculating the carrier capture rate for trap occupancy. Additionally, in equation (15), N_{tD}^{+} and N_{tA}^{-} represent the concentration of ionized donor and acceptor trap states, respectively. In brief, the occupancy of the trap states within the semiconductor depends on the mechanistic rates at which that trap either captures or emits carriers. These rates are a function of the traps' position in the energy band as well as the local Fermi level which dictates the concentration of free carriers at that point. For the electron occupancy of traps given in Equation (18), the mechanisms that will cause that trap to be occupied by an electron are the capture rate of electrons, $\bar{n}$, and the emission rate of holes, e_p. Thus, the steady state occupancy of the trap can be described as the ratio of these occupying rates to all the rates on that trap state.

Equation (18) expressing the occupancy of the localized trap state is simply a re-written form of the SRH recombination equation with the coefficients rewritten to more explicitly represent carrier emission and capture.

Additionally, Shockley-Read-Hall[54] recombination rates are used directly to model trap-assisted recombination rates using the following equation:

$$U_{SRH} = \frac{pn - n_i^2}{\tau_n \left[p + n_i \, exp\left(\frac{E_i - E_T}{kT}\right)\right] + \tau_p \left[n + n_i \, exp\left(\frac{E_T - E_i}{kT}\right)\right]} \qquad (23)$$

where U_{SRH} is the Shockley-Read-Hall recombination rate; p and n are the hole and electron concentrations; n_i is the intrinsic carrier concentration; τ_n and τ_p are the electron and hole lifetimes; E_i is in the intrinsic energy level; and E_T is the trap state energy level.

Results

Zero Bias Model

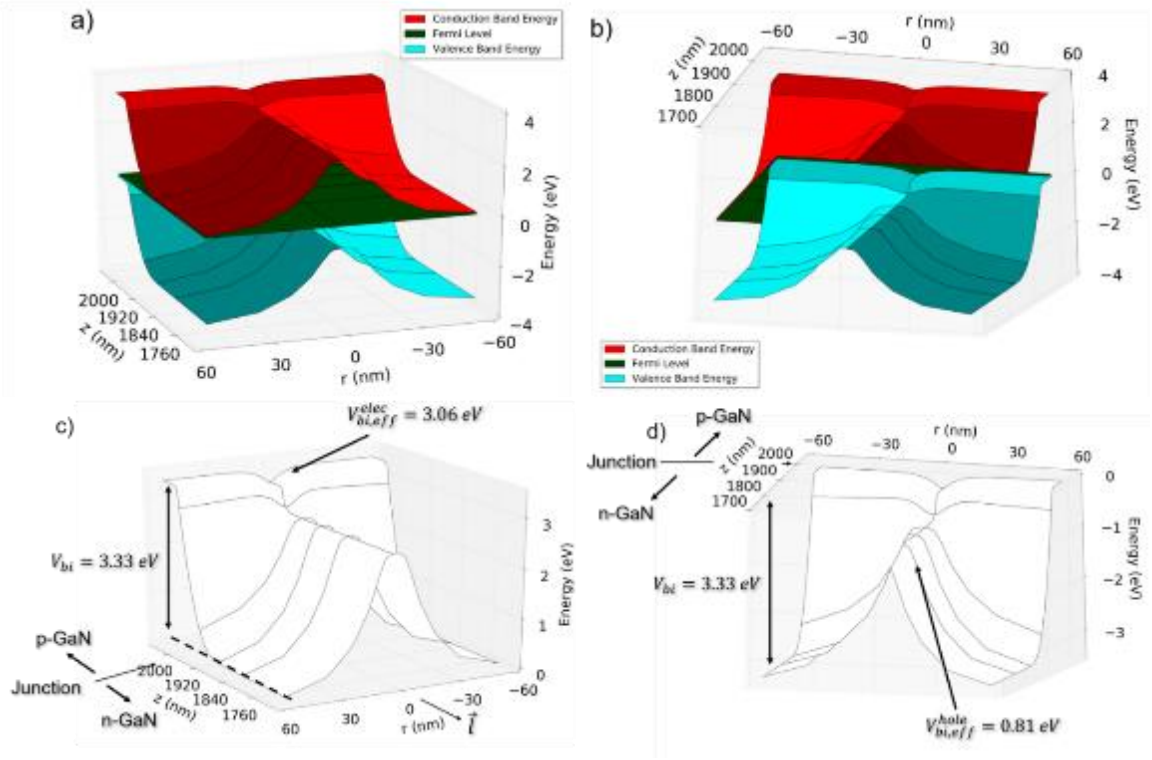


Figure 32*:* a) The full 3D zero bias band diagram of the p-n junction looking from the n-side down the dislocation line to clearly show the distortion of the band diagram around the TD line that reduces the barrier to diffusive electron current. b) The full 3D zero bias band diagram of the p-n junction rotated such that the perspective looks down the TD from the p-side. This shows more clearly the barrier to hole diffusive current and how the barriers to diffusive currents are asymmetric at the junction. c) The 3D zero bias band diagram of the p-n junction conduction band numerically annotated to demonstrate the reduction in the electron diffusion barrier around the dislocation. d) The 3D zero bias band diagram of the p-n junction valence band numerically annotated to demonstrate the marked reduction in hole diffusion barrier around the dislocation.

In Figure 32a) and b), the modeled band diagram of a GaN *p-n* junction around a TD is presented. The TD screening region permeates much further into the n-GaN region than the p-GaN region due to the screening behavior of lightly vs. heavily doped material. This reduced area of influence of the TD within the p-GaN compared to the n-GaN means that any influence

of the screening region on *p-n* junction leakage current is minimal in the p-type region of the device. Furthermore, this means that as power devices push towards lower drift region doping levels to hold large reverse voltages, the effects of the TD on the leakage associated with this screening region will similarly be amplified. It can also be seen that the band bending observed on the heavily doped p-side of the junction is substantially less than the n-side despite their trap energy levels being similarly distanced from their respective energy bands. On the p-side of the junction, the density of acceptors and trap states are on the same order of magnitude, thus there is little band bending behavior as the net charge in this region will be lower as the intentional acceptors can almost locally compensate the dislocation-related donor trap states.

In Figure 32(c) and 4(d), the contours of the conduction and valence bands respectively are shown separately from the full band diagram construction. In this construction, the asymmetry of the built-in voltage reduction on the n- and p-type sides of the junction is easier to observe. The difference in diffusion barrier height can be given by

$$\Delta V_{bi} = V_{bi} - V_{bi,eff}, \tag{24}$$

where V_{bi} is the bulk built-in potential and $V_{bi,eff}$ is the effective potential at the TD. On the n-type side, this is only 270 meV; this small reduction in the electron diffusion barrier is contrasted with the marked reduction in the barrier (2.52 eV) for holes. This result foreshadows that this structure should leak substantially more holes than electrons in forward bias since the equilibrium built-in potentials are asymmetric.

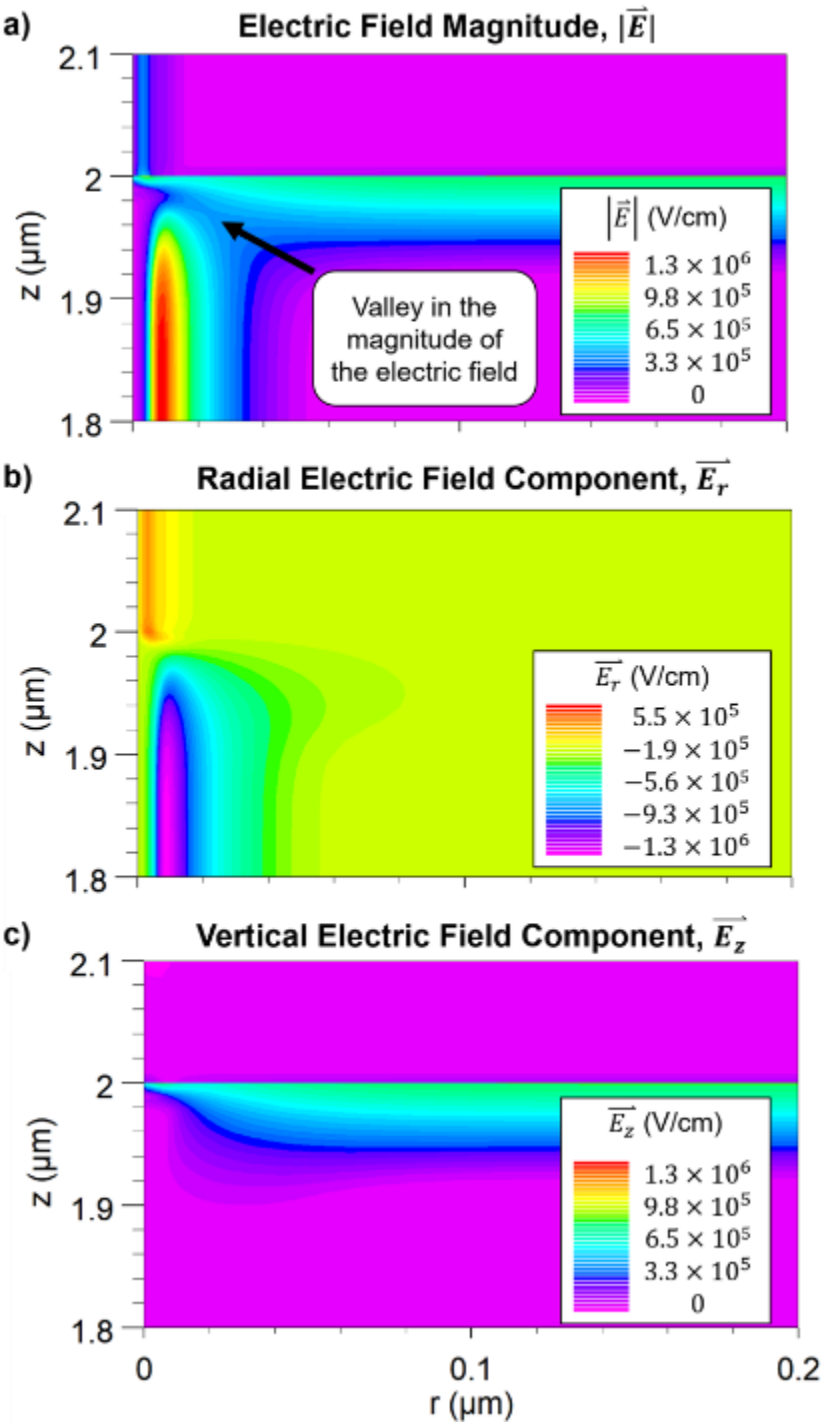


Figure 33*:* Electric field colormaps showing the a) magnitude, b) radial, and c) z-direction components. Note that at the intersection of the screening and depletion regions there is a valley in the magnitude of the electric field labeled in a). Additionally, it can also be seen that near the intersection, the electric field magnitude approaches zero where the maximum screening field would intersect with the maximum depletion electric field.

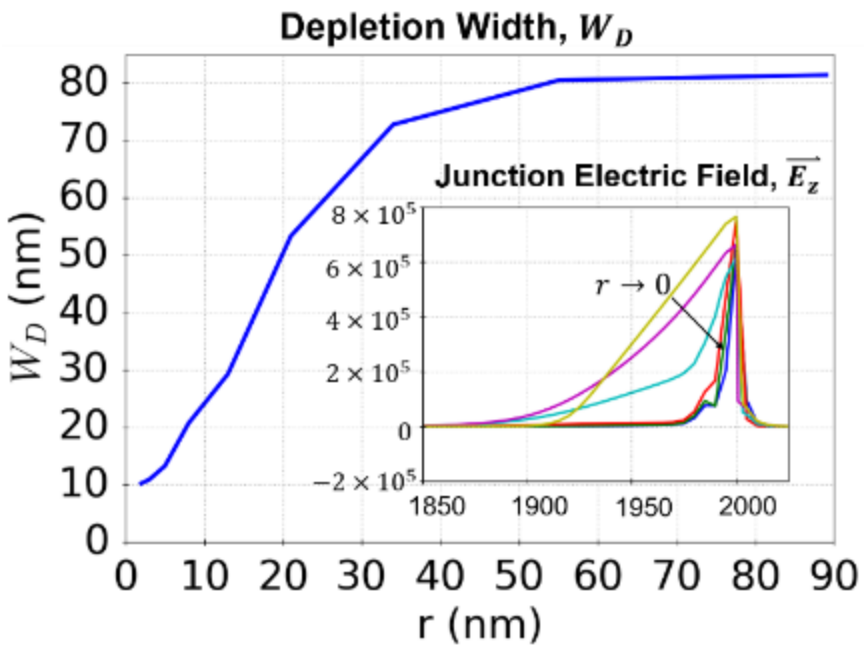


Figure 34*:* Plot of the depletion region width (calculated using the Depletion Approximation) changing with proximity to the TD core. Inset into the plot are the profiles of $\overrightarrow{E_z}$ that is responsible for the formation of the junction depletion region with different proximities to the dislocation core. Note that near the TD ($r = 0$) both the maximum $\overrightarrow{E_z}$ and depletion widths are reduced thereby creating a reduced barrier to diffusion current through this region.

In Figure 33a), the 2D electric field colormap of the zero bias *p*-*n* junction is shown. The confluence of the screening and depletion region electric fields correlates to a marked reduction in the electric field magnitude near the dislocation core. Under forward bias, this region of reduced electric field enhances the diffusive current flow as will be shown in the following section. The potential peak appears in the core of TD. Therefore, the electric field, which is the differential of potential is zero as expected.

In Figure 34, the depletion region width is plotted with respect to distance from the TD core. Near the TD, the depletion width is reduced by 67%. Furthermore, in the inset of the plot, it can be observed that the maximum junction electric field is similarly reduced by 37%. These two factors result in a substantially reduced barrier to diffusive current across the junction.

Leakage Regime (2.4V Forward Bias)

At ($V = 2.4V$), high TD density GaN *p-n* diodes have measurable leakage currents, and these currents can be reliably observed in standard computational models without problems with numerical noise.

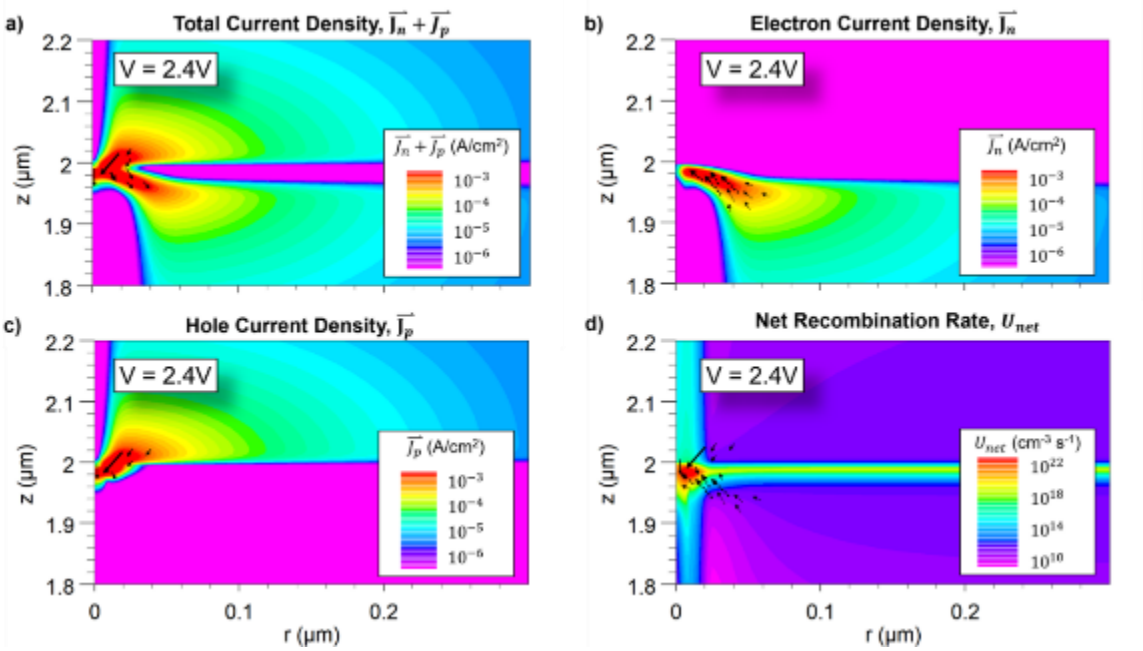


Figure 35*:* Carrier transport diagrams in the leakage regime. a) The total conduction current density for the vertical diode punctured by a threading dislocation. Note that there is current on both sides of the junction mediated by the intersection. b) The electron current density showing flow from the bulk of the n-GaN through the intersection and into dislocation trap region on the p-type side. c) The hole current density showing the flow of holes in similar magnitude to the flow of electrons. However, the holes appear to intrude much further into the n-GaN region than the electrons into the p-GaN region. d) Net recombination rate diagram showing a wide and strong area of recombination near the intersection and around the TD in the bulk. This recombination center at the intersection will be discussed further in the "Discussion" section.

In Figure 35, carrier current flow diagrams are presented. The flow of holes and electrons is almost symmetric on the p- and n-type sides of the junction, respectively. It has been previously observed at zero bias that the depletion width of the device reduces drastically with proximity to the TD, and in forward bias, this barrier reduction facilitates forward diffusive current to the

region near the intersection. With a reduction in this barrier near the TD, carriers in the bulk regions of the device bypass the bulk depletion field by moving through this region. Once both carriers are confined together in this region within the device, they will rapidly recombine (ref. Equation (23)). Lastly, it is significant to note that the hole current from the p-type side of the junction intrudes much further into the n-GaN TD than electrons into the p-GaN. This phenomenon will be discussed further in the Discussion section.

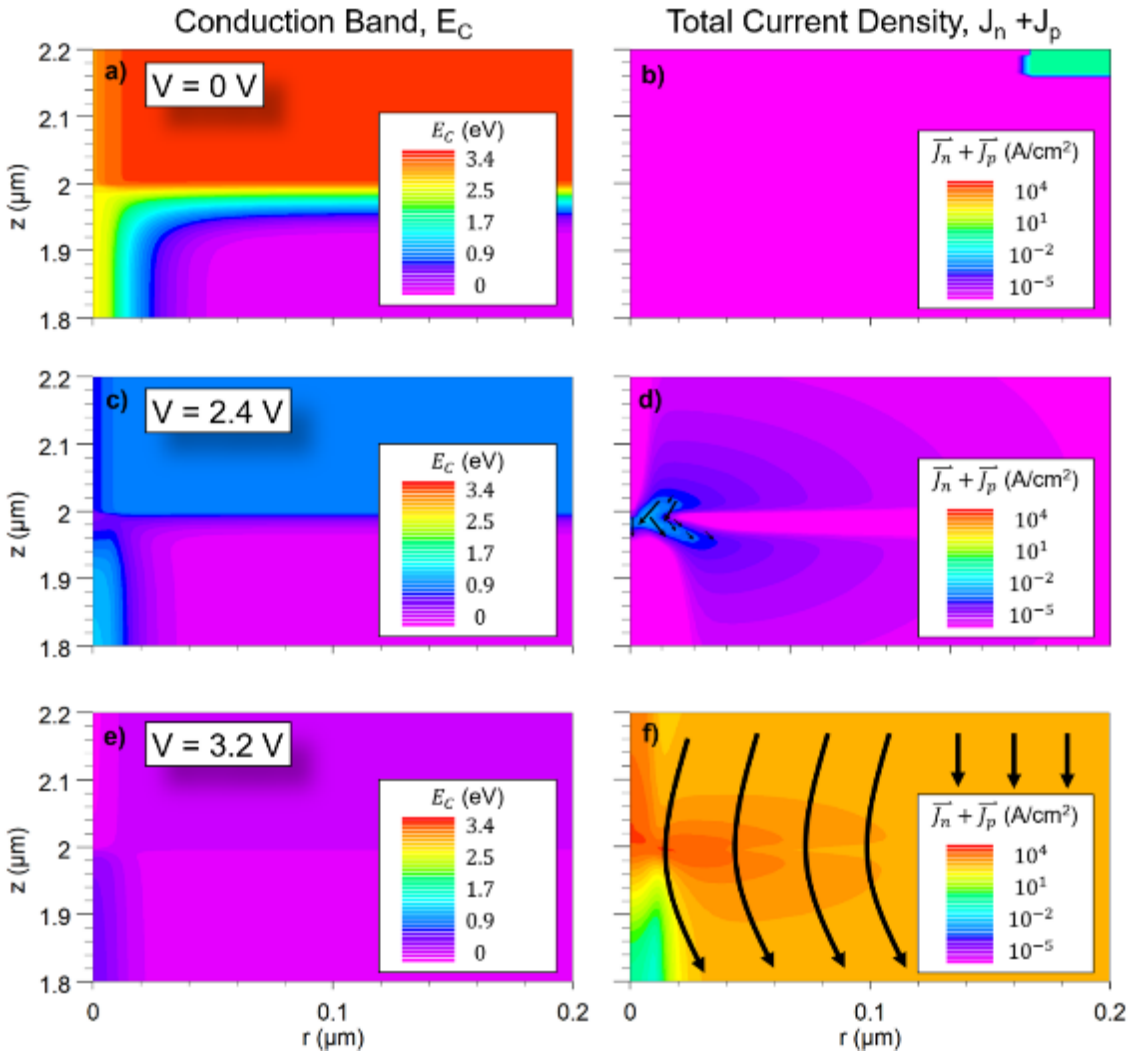


Figure 36*:* Conduction band diagrams for a) 0V, c) 2.4V, and e) 3.2V forward bias, and current density plots for b) 0V, d) 2.4V, and f) 3.2V forward bias. From these figures, note that the collapse in both the junction and screening

electric field correlates to an increase in both the junction and TD mediated currents densities until full turn-on.

In Figure 36, it can be clearly seen that the intersection mediates leakage current at sub-turn-on voltages thereby allowing current to flow through the region of reduced depletion due to the distortion in the energy band diagrams around the TD. The contrast is particularly apparent when comparing the current vectors near the TD to those far away from the dislocation at V=2.4V. Away from the TD, there is negligible current flow as would be expected in an ideal diode; however, near the TD, the current density magnitude exponentially increases as the flow of carriers moves through the region of influence of the TD.

J-V Characteristics

I-V curves were also simulated for this model and were compared to a control diode with no dislocation region. These I-V curves were normalized to a 3D model structure with cylindrical symmetry to obtain a current density (Figure 37).

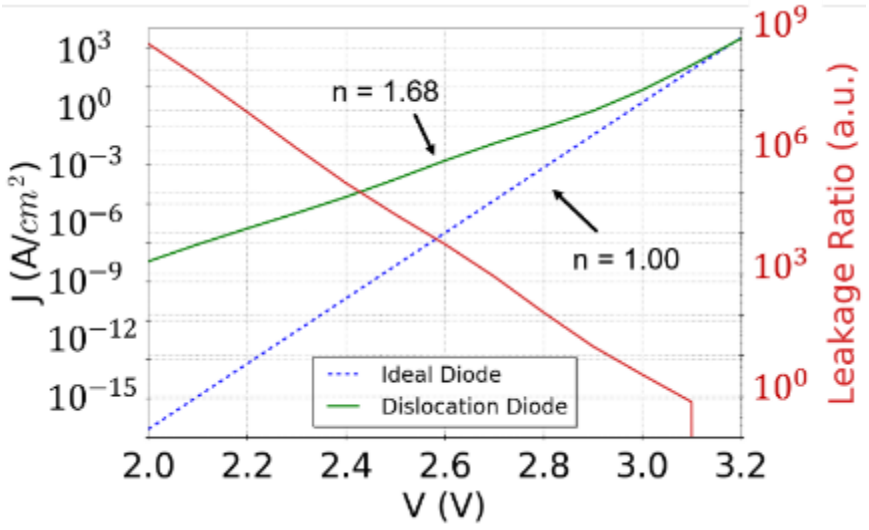


Figure 37*:* Voltage sweep analysis for the diode studied in this work against an ideal GaN *p-n* diode of the same geometry. The left axis shows the current density of the diode as well as annotations indicating the ideality factors of the diode. The right axis shows the ratio of the current in the diode with a dislocation to one without a dislocation thereby showing a leakage ratio

associated with a sample having a 10^8 cm^{-2} threading dislocation density as is typical on heteroepitaxially grown GaN-on-sapphire.

When compared to an ideal diode, the diode with the dislocation puncturing the metallurgical junction displays quantifiably higher leakage current before turn-on. After turn-on, the effects of the dislocation on the carrier transport get screened by the injected carriers at forward bias, and this effect can be seen in both the J-V curves as well as the 2D models (Figure 35).

In Figure 37, the ratio between the current densities of a diode with and without a TD is plotted with the models' J-V data using the following formula

$$\Gamma = \frac{J_{TD} - J_{noTD}}{J_{noTD}} \tag{25}$$

where Γ is the leakage ratio, J_{TD} is the current density of a *p-n* diode with a TD, and J_{noTD} is the current density of the ideal *p-n* diode. The leakage current contributes substantially more current before turn-on after which the dislocation has been screened by the forward bias current. These current ratios match very closely with previous experimental work analyzing leakage current in vertical *p-n* junctions in GaN[36].

Discussion

Pinning Behavior at the Dislocation

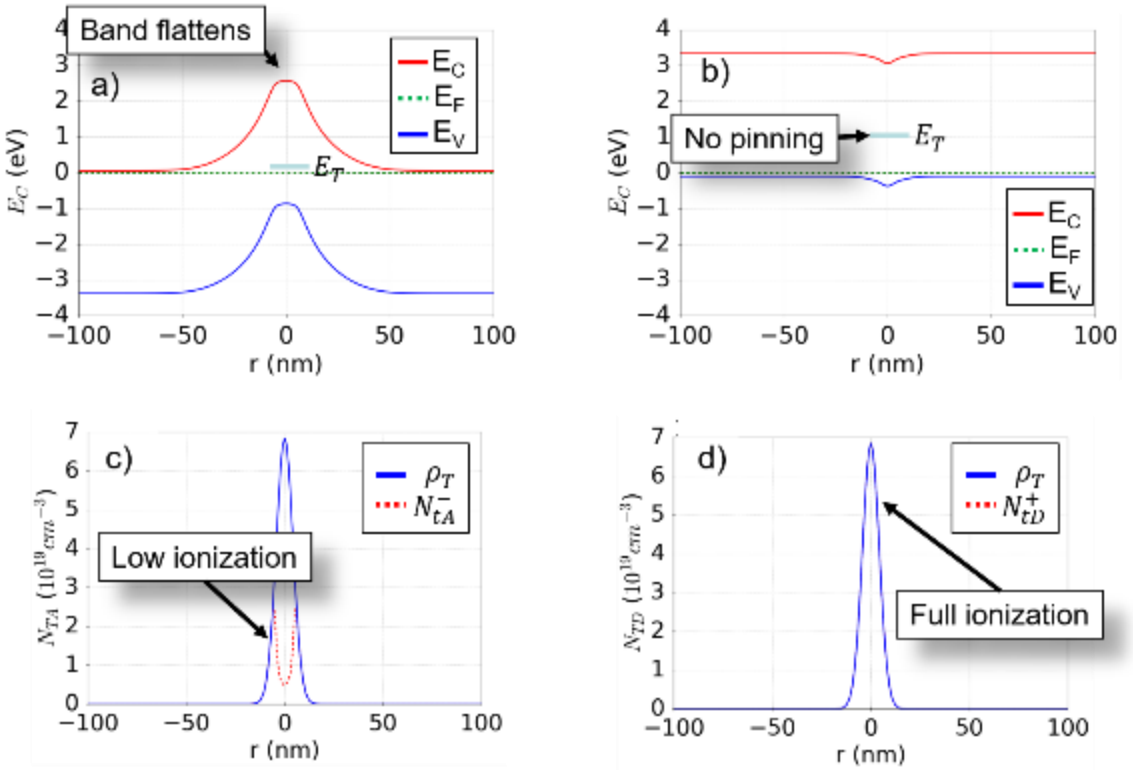


Figure 38: Band diagrams for a) lightly-doped n-GaN and b) heavily-doped p-GaN around a TD. In the bottom row are also shown the charge densities for c) lightly-doped n-GaN and d) heavily-doped p-GaN. Note that in the lightly-doped n-GaN, the band flattens near the dislocation indicating a very low electric field and reflecting a low occupancy as also indicated in the charge density graph in c).

Our results demonstrate that the previously observed small potential profiles around TDs in p-GaN[28] are due to the necessary doping required to obtain p-type conduction. Since the concentration of acceptors in p-type GaN ($N_A = 5 \times 10^{19}\ cm^{-3}$) are on the order of trap state density near the dislocation core ($\rho_{T,max} = 6.84 \times 10^{19}\ cm^{-3}$), the net charge in the TD region in p-GaN is less than the net charge in the n-GaN where the donor concentration is much smaller ($N_D = 5 \times 10^{17}\ cm^{-3}$). This reduction in the net charge density in p-GaN directly

correlates to the reduction in the associated dislocation band bending around those dislocations and results in a 100% hole occupancy of the dislocation-related trap states. It is significant to note that the trap states in the lightly doped n-GaN region of the diode are not fully occupied near the TD thus causing the hump in the charge concentration profile, as shown in the lower left corner of Fig. 10.

Furthermore, our results also demonstrate that the lightly doped, n-type side of the p-n junction does not actually physically pin the Fermi level at the trap state either. The low donor concentration is physically unable to compensate the trap states without bending the bands such that the trap state remains at or below the Fermi level. Although graphical representations appear to have the trap state pinned at the Fermi energy, it is in fact 67 meV above the trap energy level. Using Fermi statistics,

$$f(E) = \frac{1}{\exp\left(\frac{E_T - E_F}{kT}\right) + 1}, \tag{26}$$

it can be calculated that the occupancy of a trap state located 67 meV above the Fermi level will be ~8% which matches the occupancy given by the model.

Major Mechanisms of Leakage

The results presented clearly demonstrate a strong leakage mechanism at the intersection where the dislocation and metallurgical junction interact; however, additional studies are necessary to fully verify the effect of lightly doped regions with TDs on p-n junction leakage.

Leakage in n+ - p Diode

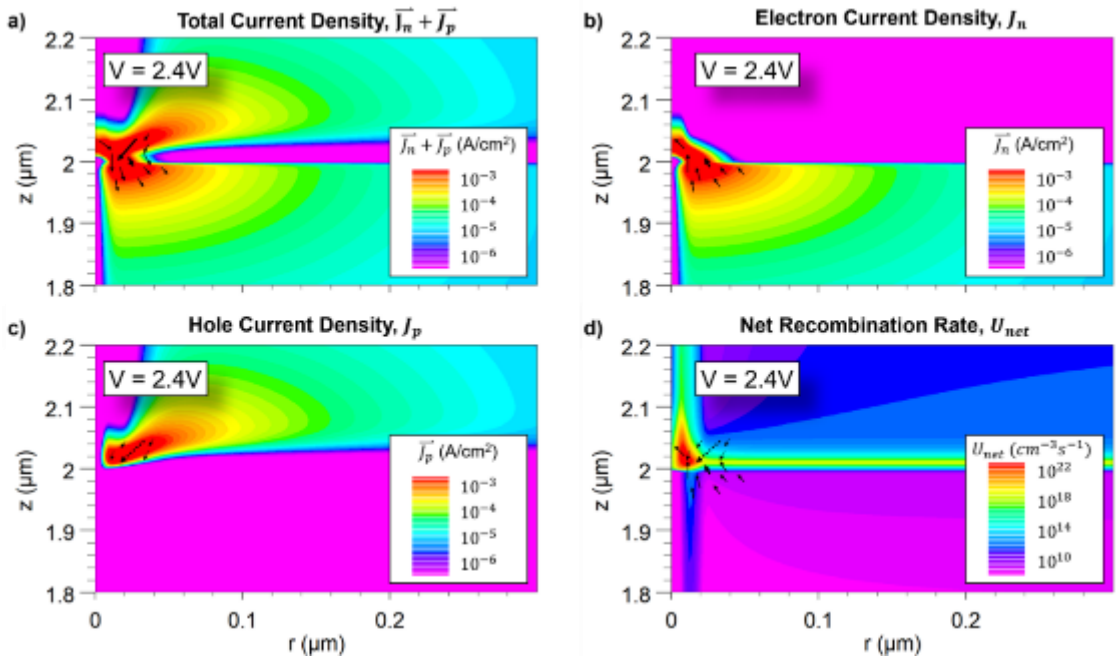


Figure 39: n+ - p diode leakage current and recombination profiles. All plots are plotted using a log scale with the same magnitudes given in previous current density figures. a) Total current density, b) electron current density, c) hole current density, and d) net recombination rate.

The first exploratory model inverted the weight of the doping to create a n+ - p junction rather than the p+ - n junction. This model verified that it is the lightly doped region of the diode that mediates the most leakage; in **Figure 39**a), the TD on the p-type side (which is now lightly doped with $N_A = 5 \times 10^{17}\ cm^{-3}$) carries a significant amount of electron current with the same partial occupancy and band flattening behavior observed in our main model. Furthermore, this current goes substantially further into the p-type region through the TD which indicates that carriers in these regions are more likely inhibited by their mobility as would be predicted if they were acting as majority carriers in these regions.

p-GaN Trap State Energy Dependence

As was previously stated, the precise location of the trap energy level for TDs in p-GaN is not known, thus models looking at p-n junctions with different p-GaN TD trap energy levels were simulated. It was observed that the trap state level of the p-type side was largely irrelevant to the presence of the previously observed leakage mechanisms. This finding indicates that although the energy level for TD traps in p-GaN is approximated as a deep trap state, its location within the band ultimately does not matter since one side of the junction trap states are deep and distort the band structure to allow the leakage mechanisms to occur. This result further reinforces the notion that if the acceptor concentration is on the order of the trap state concentration, they play a much more significant role than the trap state energy in determining the bending behavior around the TD.

Trap-Assisted Recombination Dependence

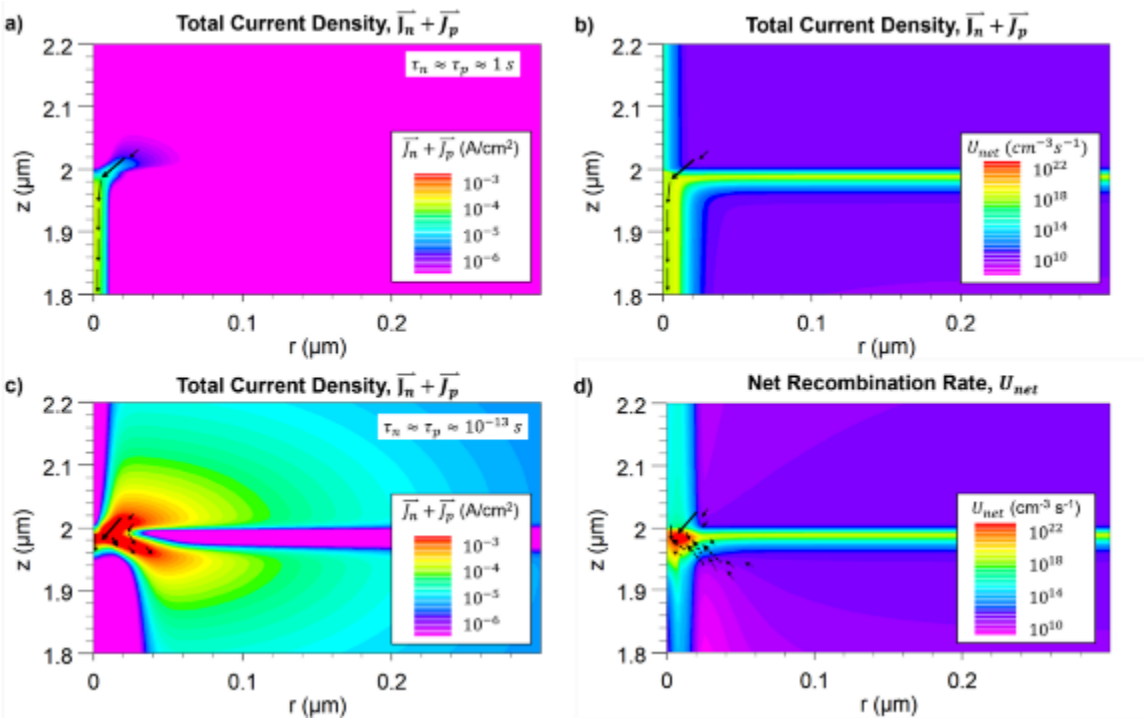


Figure 40: Total current density color maps highlighting the effect that the explicit, dislocation trap mediated carrier recombination has on the leakage current magnitude. a) Total current density colormap of the diode with a 1s carrier lifetime (thereby negating recombination effects of the dislocation trap states). Note that even without any trap state recombination, the dislocation screening region on the lightly doped side of the junction continues to mediate leakage current. b) Total current density colormap of the control diode with 1fs carrier lifetime.

Previous models have indicated that the leakage mechanism around TDs are related to carrier recombination near the intersection as shown by disk-shaped regions of high recombination rates in Figure 35 and **Figure 39**. To test this, a model with trap-associated lifetimes of 1s was simulated to nullify the effect of trap state recombination at the interface. As can be seen in Figure 40, the removal of SRH recombination at TD trap states does not completely remove leakage currents, but it does reduce them by almost an order of magnitude. In addition to the SRH recombination at the interface near the TD, the diffusion current of the

junction alone near the TD also provides leakage current well over what would be expected in a perfect p-n diode. This effect can further be seen in **Figure 41**. Although the SRH recombination at the TD trap states appears to have a significantly high leakage current in **Figure 40**, **Figure 41** shows that the leakage current is largely caused by the depletion region and diffusion barrier reduction effects around the TD, for the leakage ratio of the no TD recombination diode over the ideal diode is approximately 10^4 at V = 2.4V compared to 10 between the Control and the no TD recombination diode. With the absence of recombination at the trap states, the diffusive current component of the Drift-Diffusion current model

$$\overrightarrow{J_n} = qn\mu_n\overrightarrow{E_n} + \boldsymbol{qD_n\nabla n}, \tag{27}$$

is still greater than the drift component thereby allowing leakage current to flow. However, the drift current still reduces the overall current by repelling carriers away from the intersection. By adding in trap state recombination, the drift component of the model becomes irrelevant as carriers do not need to fully cross the depletion region. Instead, they simply need to overlap with the carriers diffusing from the other side of the junction at which point they rapidly recombine and create a much higher leakage current mediated by the depletion and barrier reduction and enhanced by the trap state recombination.

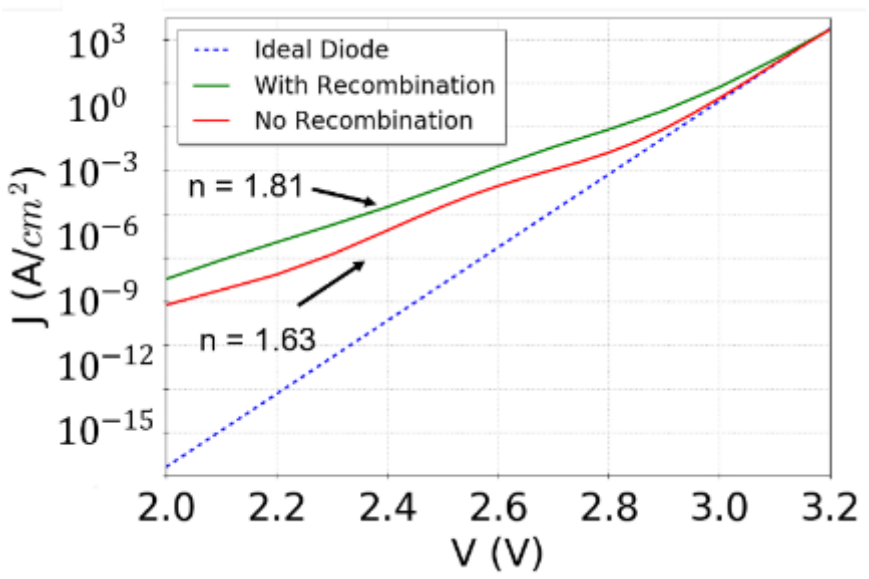


Figure 41: J-V curves comparing the ideal, control, and no recombination diode models.

Isolated Screening Region Geometry Dependence

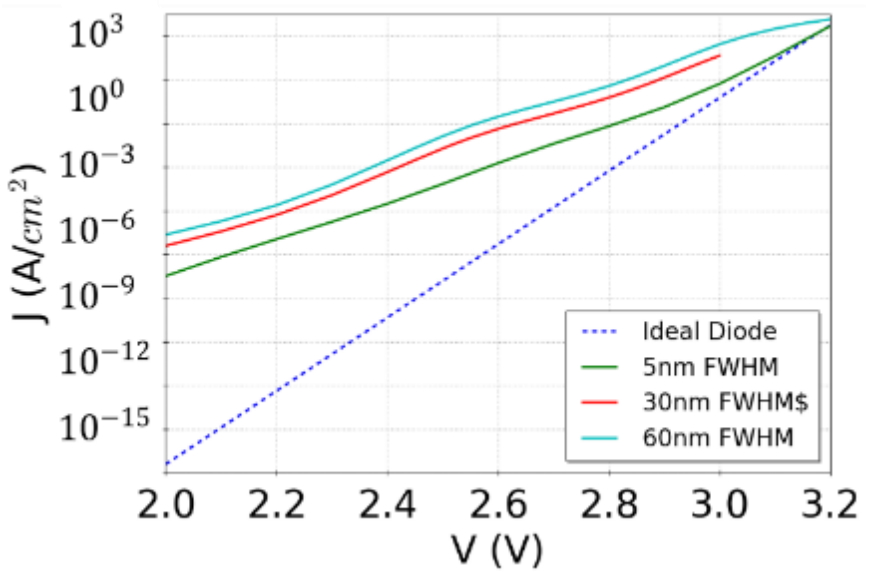


Figure 42: J-V curves contrasting the effects of only the trap state distribution (hence screening region length) on the leakage current. This study differentiates the effects of only the screening geometry without changing the dislocation line charge or device doping.

In addition to exploring the effect of screening region variance by controlling the doping in the junction, the screening region was also modified by changing the density profile of the TD-associated traps. These Gaussian FWHMs were modified to make them broader, but the peak trap state densities were also changed such that an experimentally observed one electron per c-lattice translation was maintained. In Figure 42, the J-V curves of these broader trap state models are shown, and it can be clearly observed that the width of the distortions does contribute significantly to the forward bias leakage current.

With the reduced trap state densities, the effects previously seen on the trap occupancy in the lightly doped region of the diode are eliminated, yet leakage current not only persists but increases substantially. This indicates that the occupancy of the trap states does not play a major role in facilitating leakage since the trap states are fully occupied for these cases. Furthermore, in **Figure 43**, we can see that the local magnitude of the leakage currents remains relatively unchanged with broader screening regions even as the total device current density increases. This indicates that the broader screening region interaction with the junction simply broadens the region over which diffusion current and SRH recombination can occur.

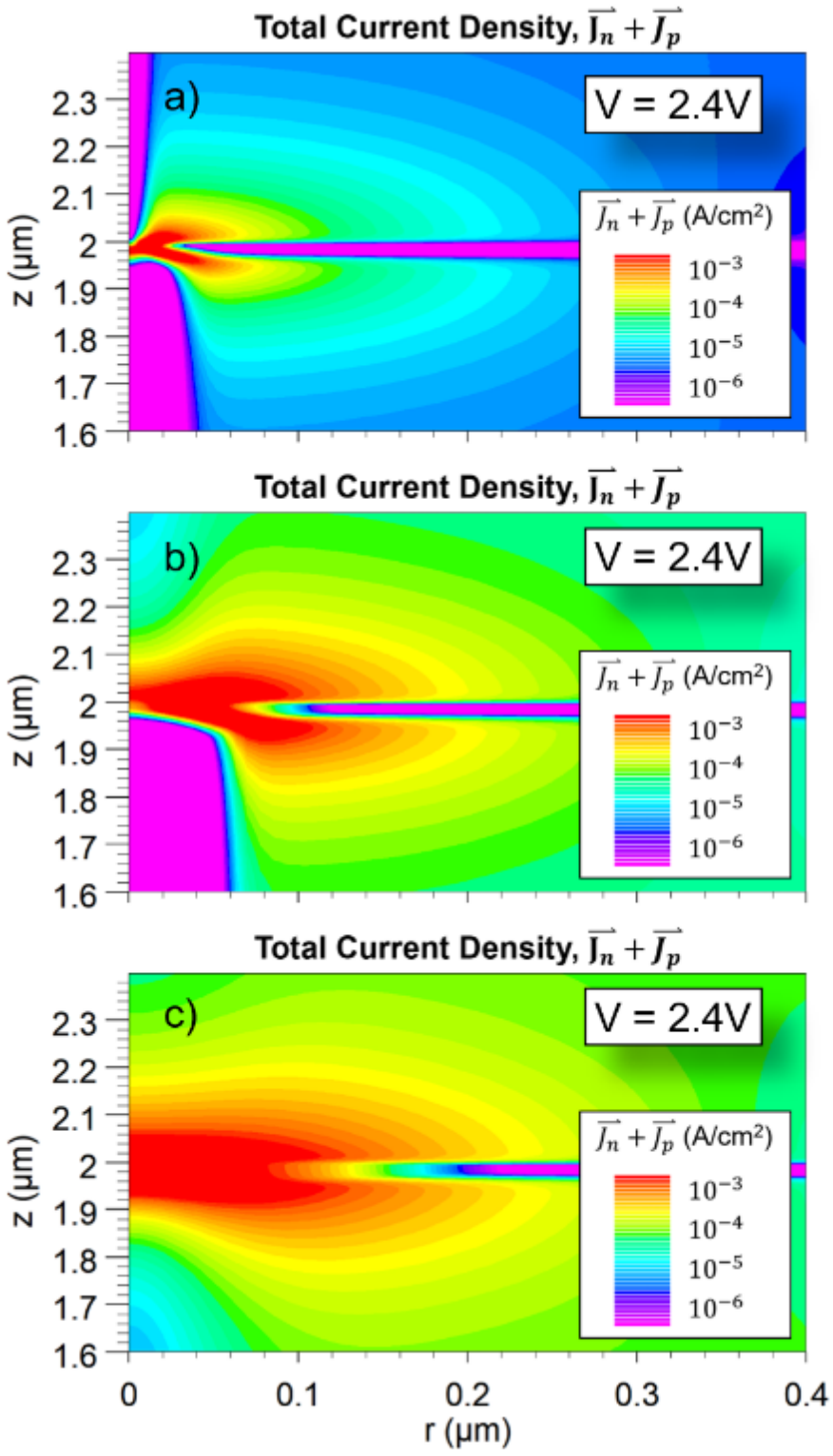


Figure 43: Conduction current densities for various FWHM TD trap distributions with a) the main model with a FWHM = 5nm, b) a FWHM = 30nm, and c) a FWHM = 60nm.

Summary

This work has presented a 2D model of a *p-n* diode punctured by a distribution of trap states associated with dislocations in accordance with prior investigations[29,55] and solved the Poisson-Drift-Diffusion system of equations using the Gummel method to determine the mechanisms by which dislocations mediate leakage. It was discovered that the dislocation trap states were ionized by the surrounding dopants thus distorted the band in their vicinity with a heavy dependence on the doping density. This distortion of the energy bands results in a drastically reduced barrier to diffusion in forward bias, and this reduced diffusion barrier allows carriers to flow into a region of incredibly high recombination rates. It was discovered that regions around TDs in lightly doped semiconductors also inverted their majority carrier behavior which allowed leaked carriers to travel very far into lightly doped region through the TD. The regions of barrier reduction, SRH recombination, and majority carrier inversion created by the distortion in the band structure results in observable leakage currents and increased ideality factors in GaN *p-n* junctions with dislocations.

This article has been submitted for publication to the Journal of Applied Physics.

Dislocation Mediated Reverse Bias Leakage

Introduction

III-N semiconductors have been widely used in high-speed transistors[1–5], visible and ultraviolet (UV) optoelectronics[6–12], and vertical power electronics[13–17]. The high theoretical breakdown field (~3.3 MV/cm) and carrier mobility (>1,000 cm^2/V-s) have garnered interest in the field of power electronics where energy efficiency and high voltage operation are necessary. Vertical device topologies are useful for reducing the wafer footprint of power electronics by allowing voltage to be held across epitaxially grown interfaces rather than lateral

ones. One of the major challenges to the performance of GaN vertical power devices has been the ubiquitous presence of threading dislocations (TDs) in the substrates for epitaxial growth. TDs have been repeatedly shown to exacerbate breakdown modes such as reverse bias current leakage in vertical GaN devices[16,18,19], but the breakdown mechanisms have been hitherto unstudied despite being experimentally observed.

The dislocation structure in GaN has been extensively studied by high-resolution x-ray diffraction (HRXRD) and transmission electron microscopy (TEM). Edge and mixed-type threading dislocations have been shown to be much more prevalent than their screw-type counterparts, but they all have a line vector within ~10° of the <0001> direction regardless of their Burger's vector, $\vec{\boldsymbol{b}}$ [20,21]. Furthermore, the electrical nature of TD trap states in n-GaN has been shown to be a deep acceptor in the band gap with a line density of approximately one electron trap state per c-lattice translation. It has also been observed that this trap state density associated with TDs results in a screening region around the dislocation as the donors provide electrons to the trap states to create regions of significant net charge. In a simple picture, the occupied dislocation-related acceptors in n-type material are screened by ionized donors as shown in Figure 29. Similarly, we assume that dislocation-related donors are screened by ionized acceptors in p-type material.

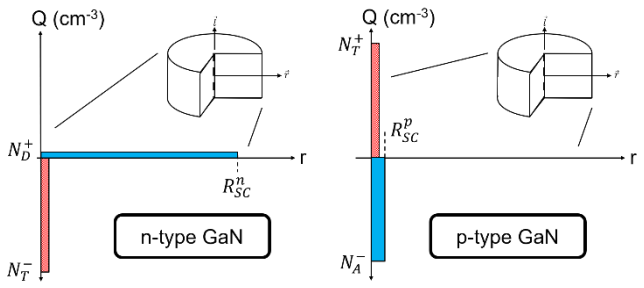


Figure 44: Simplified representation of screening regions around a dislocation in a lightly doped (N_D= 5×10^{17} cm^{-3}) n-type (left) and heavily doped (N_A= 5×10^{19} cm^{-3}) p-type (right) GaN. Note that the charge region around the

dislocation in p-type GaN is much smaller than in n-type GaN due to the high doping required to produce p-type conductivity being on the order of the density of trap states.

In the simplest treatment, the dislocation and space charge regions are cylindrical with constant trap state and dopant density (Figure 29). The screening radius can be simply calculated using charge neutrality and results in

$$R_{SC} = \sqrt{\frac{\rho_n}{\pi c}} * \sqrt{\frac{1}{N}} \qquad (0)$$

where ρ_n is the number of trap states per c-lattice translation, c is the c-lattice constant, and N is the uniform dopant concentration of the semiconductor. This ionization and screening of the cylindrical area of the TD line distorts the energy band profiles around the dislocation with potentials of ~2.5 V as observed by electron holography in n-GaN[22]. This behavior has been attributed to the coalescence of defects around the TD core as suggested by Arslan and Browning[23] and observed by Müller et al.[24]. The trap state energy associated with such a band bending closely matches an electron trap state ~1.0 eV above the valence band maximum found in DLTS measurements[25]; additionally, the trap state density are consistent with previous experimental and theoretical values of approximately one electron trap state per c-lattice translation[26]. From these experimental observations and theoretical predictions, it is possible to construct an accurate band structure model of n-type GaN pierced by a TD.

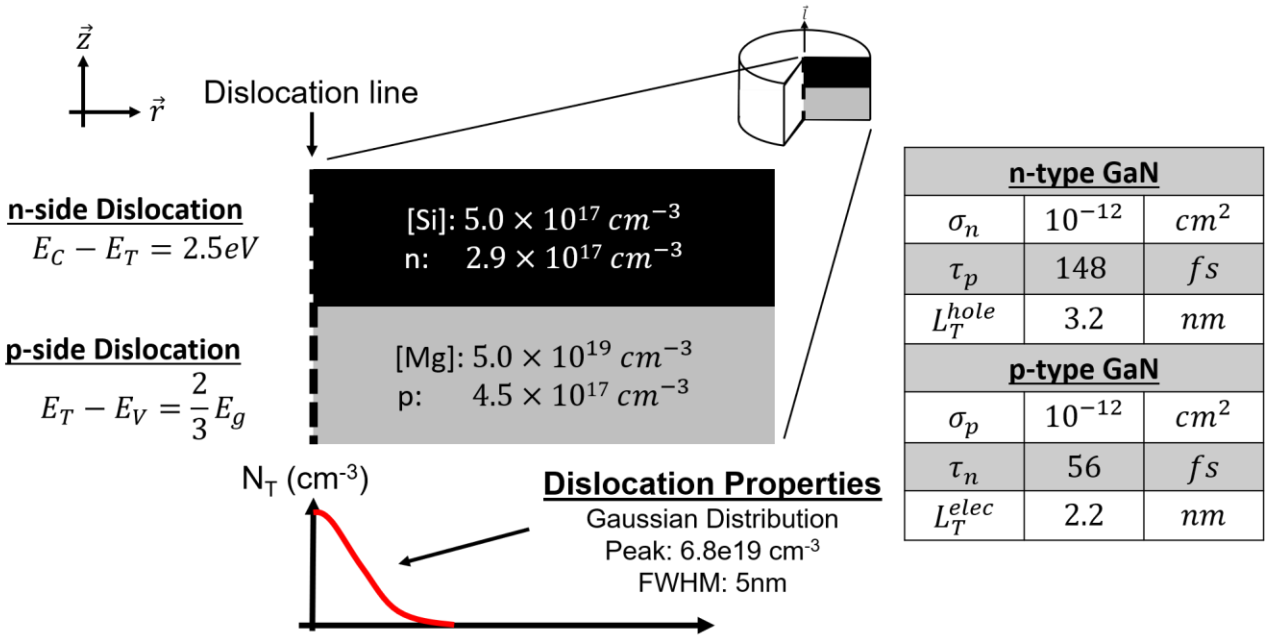
In contrast, a band structure model of p-type GaN that includes the treatment of TD trap states has been substantially more elusive. Electron holography analyses have found regions of negative space charge that is likely associated with screening acceptors around a donor trap states coalescing near TDs in p-GaN[22]. However, the high acceptor concentration (needed to achieve measurable hole conductivity) results in a screening region that is smaller than the resolution of the electron holography method (~2 nm). Thus, the nature of the TD charge

behavior in p-GaN remains experimentally unobserved. However, in our previous work, TDs in p-GaN act as nonradiative centers similar to n-GaN as shown by cathodoluminescence (CL) results[27], thus we assume that the TD trap states behave similarly in p- and n-type GaN.

In our previous work, GaN p-n diodes with a single threading dislocation were modeled in forward bias. It was found that the band distortions observed in the unipolar regions experimentally result in a reduced diffusion barrier for carriers to bypass the built-in potential of the diode thereby mediating a diffusive leakage current in forward bias. In this work, we will use the same simulation system with an additional mathematical model to address dislocation-mediated reverse bias leakage currents.

Model

In Appendix A, all relevant variables are given in alphabetical order to assist in understanding the parameters and models used in this work.



n-type GaN		
σ_n	10^{-12}	cm^2
τ_p	148	fs
L_T^{hole}	3.2	nm
p-type GaN		
σ_p	10^{-12}	cm^2
τ_n	56	fs
L_T^{elec}	2.2	nm

Figure 45. A cylindrically symmetric pn diode is modeled for this study with a Gaussian distribution of deep trap states used to represent the TD-associated traps. Typical doping densities for the p- and n-type regions are used, and experimentally common hole and electron concentrations are observed in the

model. The location of the trap state energy within the n-type region was based on experimental results while the p-type region was placed arbitrarily deep in the energy gap. In the right table, values for trap capture cross section (σ), minority carrier lifetime (τ), and minority carrier diffusion length (L_T) are given for the trap state region associated with the TD line. These values were chosen such that these model variables all matched experimental values as closely as possible.

In this study, Silvaco's ATLAS modeling software was used to solve for the 2D pn junction model shown in Figure 30. Cylindrical coordinates were used to simplify the computational requirements by utilizing the six-fold rotational symmetry of the 3D crystal structure about the TD line vector, <0001>, without resorting to a full 3D treatment. N_A and N_D values are chosen based on experimentally typical values for vertical GaN *p-n* junctions doped with Mg and Si, respectively. The model r-dimension limit of 564 nm approximates a 10^8 cm^{-2} TD density as is typical in commercially available GaN growth on either Al_2O_3 or SiC. Our TD-associated trap state region was treated as a Gaussian distribution with FWHM of 5 nm and a peak trap state density of 6.84×10^{19} cm^{-3}. This distribution approximates a one electron per c-lattice translation when normalized in the z-direction. Trap energy levels within the bandgap were E_C – 2.5 eV and E_V + 2.3 eV for n- and p-type GaN, respectively. Although the energy level of the dislocation trap state in n-GaN is well-documented, the level for p-GaN is approximated as an arbitrarily deep donor state. This assumption will be discussed later.

The trap state properties are also chosen such that the minority carrier diffusion lengths and lifetimes match those given in the literature. Using the approximation of a 10^{16} cm^{-3} trap state density in the bulk regions away from the dislocation, a capture cross section for both electrons and holes of 10^{-12} cm^2 was chosen based on the following equations:

$$\tau = (\rho_T * \sigma * \nu)^{-1} \tag{28}$$

$$L_T = \sqrt{\frac{kT}{q} * \mu * \tau}, \quad (29)$$

where τ is the minority carrier lifetime; ρ_T is the local trap concentration; σ is the trap minority carrier capture cross section; v is the minority carrier thermal velocity; L_T is the minority carrier diffusion length; and μ is the minority carrier mobility. These values resulted in a lifetimes and diffusion lengths given in Table 8 using the minority carrier mobilities found by Kumakura et al.[28]. The bulk values given in this table are within the expected range for minority carrier diffusion length and lifetime[28–31] and were observed in our diode model with no dislocation.

	$\rho_T\ (cm^{-3})$	τ_n	$L_T^{elec}\ (nm)$	τ_p	$L_T^{hole}\ (nm)$
TD core	6.84×10^{19}	56 fs	2.1	148 fs	3.2
Bulk	10^{16}	0.38 ns	178	1.01 ns	261

Table 9: Minority carrier lifetimes and diffusion lengths for different trap state conditions. The bulk lifetimes are within experimental parameters for minority carrier lifetimes[28].

Using this physical model, a mesh is constructed with a radial dimension of 0.564 μm to approximate the 10^8 cm^{-2} TDD and a vertical dimension of 4 μm with the metallurgical junction at 2 μm. The resolution of the mesh varies from 1 Å near the junction and dislocation to 50 nm in the bulk. The Poisson and steady-state Current Continuity equations are solved on our mesh self-consistently using the Gummel method (Figure 31).

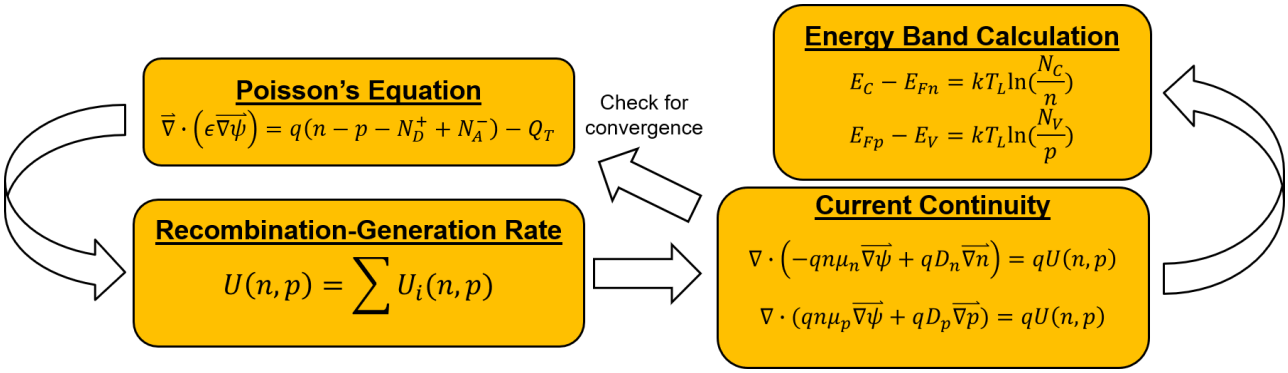


Figure 46. Process overview the Gummel method which was used extensively for modeling dislocation behavior; however, the Newton-Raphson methodology was used if convergence was not achieved.

$$\vec{\nabla} \cdot \left(\epsilon \vec{\nabla} \psi\right) = q(n - p - N_D^+ + N_A^-) - Q_T \tag{30}$$

$$\nabla \cdot \overrightarrow{J_n} = -qU(n,p) \tag{31}$$

$$\nabla \cdot \overrightarrow{J_p} = qU(n,p) \tag{32}$$

In the Poisson equation (10), ψ is the electric potential; n and p are the electron and hole concentration; N_D^+ and N_A^- are the ionized donor and acceptor concentrations. In the Current continuity equations, $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, and $U(n, p)$ is the net recombination-generation rate. If convergence is not achieved, the solver will switch from the Gummel to the Newton-Raphson method to solve the system of equations.

In addition to these core equations, additional models are necessary to include the various behaviors of the GaN material systems and trap physics. These are discussed below.

Incomplete Ionization Model

It has been well-documented experimentally that Mg_{Ga} has an activation energy around 190 meV[32], thus to accurately model p-GaN, we utilized the incomplete ionization model[33] to account for the thermal activation of both the donors and acceptors in GaN.

$$N_D^+ = \frac{N_D}{1 + g_n exp\left(\frac{E_{Fn} - (E_C - E_D)}{kT}\right)} \tag{33}$$

$$N_A^- = \frac{N_A}{1 + g_p \exp\left(\frac{(E_A - E_V) - E_{Fp}}{kT}\right)}, \tag{34}$$

where N_D^+ and N_A^- are the ionized donor and acceptor concentrations; N_D and N_A are the donor and acceptor concentrations; g_n and g_p are the conduction and valence band degeneracies; E_{Fn} and E_{Fp} are the electron and hole quasi-Fermi levels; $(E_C - E_D)$ and $(E_A - E_V)$ are the donor

and acceptor activation energies. This model predicts that only ~1% of the Mg acceptor dopants will contribute holes to the GaN semiconductor while ~60% of the Si donors will contribute electrons. Furthermore, unintentionally-doped GaN is usually slightly n-type due to the unintentional doping by oxygen. This combined with the low activation efficiency necessitate high Mg concentrations to experimentally realize p-type GaN.

Our model makes two basic doping assumptions. Firstly, the model uses an abrupt metallurgical junction such that there is no overlap between the p- and n-type regions of the diode. Secondly, the model does not explicitly specify any compensating defects or recombination centers away from the dislocation but rather combines the all real crystal imperfections into a minority carrier lifetime within the range of values provided in the literature[28].

Shockley-Read-Hall (SRH) Trap-Assisted Recombination Model

To model the charging and screening effects around the dislocation line, a trap ionization model was implemented. The Simmons and Taylor model (based on Shockley-Read-Hall recombination statistics)[34–36] was used to simulate the occupancy, $f(E_T)$, and charge state density of trap states, Q_T, associated with the TD line:

$$Q_T = q(N_{tD}^{+} - N_{tA}^{-}) \tag{35}$$

$$N_{tA}^{-} = \rho_T * f(E_T) \tag{36}$$

$$N_{tD}^{+} = \rho_T * (1 - f(E_T)) \tag{37}$$

$$f(E_T) = \frac{\bar{n} + e_p}{e_n + \bar{n} + \bar{p} + e_p} \tag{38}$$

$$\bar{n} = \nu_n \sigma_n n \tag{39}$$

$$\bar{p} = \nu_p \sigma_p p \tag{40}$$

$$e_p = \nu_p \sigma_p N_V \exp(\frac{E_V - E_T}{kT}) \tag{41}$$

$$e_n = \nu_n \sigma_n N_C \exp(\frac{E_T - E_C}{kT}) \tag{42}$$

In this system of equations, Q_T is the concentration of charged trap states; N_{tD}^{+} and N_{tA}^{-} are the concentration of ionized donor and acceptor trap states; ρ_T is the density of trap states, $f(E_T)$ is the Fermi occupancy function at the trap state energy level; $\bar{n}$ and $\bar{p}$ are the electron and hole capture rates; ν_n and ν_p are the thermal velocities for electrons and holes; σ_n and σ_p are the electron and hole capture cross sections; n and p are the electron and hole concentrations; e_p and e_n are the hole and electron trap emission rates; N_V and N_C are the effective density of states for the valence and conduction bands; E_V and E_C are the valence and conduction bands; and E_T is the trap state energy level. These equations tie into the previous models given in two important ways. First, the electron and hole concentrations given in (19) and (20) depend on the carrier quasi-Fermi levels. In forward bias, these quasi-Fermi levels split near the junction and would therefore change the behavior of the traps in these regions. This change carrier statistics in the regions with Fermi level splitting is considered in these two equations by the inclusion of the local carrier concentrations which depend on the quasi-Fermi levels. Second, as previously stated, the trap states are given a capture cross section such that the minority carrier lifetimes and minority diffusion lengths in the bulk associated with a lower concentration of these traps matches with previously found experimental evidence. The chosen values for capture cross section also come into effect here when calculating the carrier capture rate for trap occupancy. Additionally, in equation (15), N_{tD}^{+} and N_{tA}^{-} represent the concentration of ionized donor and acceptor trap states, respectively. In brief, the occupancy of the trap states within the semiconductor depends on the mechanistic rates at which that trap either captures or emits carriers. These rates depend on the traps' position in the energy band as well as the local Fermi level which dictates the local free carrier concentration. For the electron occupancy of traps given in Equation (18), the mechanisms that will cause that trap to

be occupied by an electron are the capture rate of electrons, $\bar{n}$, and the emission rate of holes, e_p. Thus, the steady state occupancy of the trap can be described as the ratio of these occupying rates to all the rates on that trap state.

Equation (18) expressing the occupancy of the localized trap state is simply a re-written form of the SRH recombination equation with the coefficients rewritten to more explicitly represent carrier emission and capture.

Additionally, Shockley-Read-Hall[36] recombination rates are used directly to model trap-assisted recombination rates using the following equation:

$$U_{SRH} = \frac{pn - n_i^2}{\tau_n \left[p + n_i \, exp\left(\frac{E_i - E_T}{kT}\right)\right] + \tau_p \left[n + n_i \, exp\left(\frac{E_T - E_i}{kT}\right)\right]} \qquad (43)$$

where U_{SRH} is the Shockley-Read-Hall recombination rate; p and n are the hole and electron concentrations; n_i is the intrinsic carrier concentration; τ_n and τ_p are the electron and hole lifetimes; E_i is in the intrinsic energy level; and E_T is the trap state energy level.

Trap Assisted Tunneling

In addition to these core equations and the models outlined above for general GaN p-n junction, the Trap-Assisted Tunneling model[37,38] was also included for the purposes of simulating reverse bias leakage currents in the presence of a high electric field. In this model, an additional recombination-generation term

$$U_{TAT} = \frac{q m^* \left|\vec{E}\right| M^2 g_T \rho_T}{8\pi\hbar^3 (E_T - E_V)} \exp\left(-\frac{4\sqrt{2m^*(E_T - E_V)^3}}{3q\hbar\left|\vec{E}\right|}\right) \qquad (44)$$

is included in Equations (31) and (32). In this model, U_{TAT} is the trap-assisted tunneling net recombination-generation rate, q is the electron charge, m^* is the effective mass of the carrier, $|\vec{E}|$ is the magnitude of the local electric field, M^2 is the matrix element for the trap potential[39], g_T is the degeneracy of the trap states, ρ_T is the density of trap states, $\hbar$ is Planck's constant,

and E_T is the trap state energy level. Note that the electric field magnitude is located in both the numerator outside the exponent and in the denominator of the argument of the exponent – this means that as the electric field magnitude increases at each mesh point, the exponential will converge to 1 while the outside multiple will increase linearly, thus for the purposes of this work where the electric fields are very large, the net recombination-generation rate is approximately linearly related to the electric field magnitude. This model accounts for the net recombination-generation of carriers across the band with the assistance of trap states with negative values of U_{TAT} correlating to a net generation of carriers.

Results

Before discussing reverse bias results, we first confirmed that our zero bias band diagram with the additional physical models added matched our band diagram in previous work on forward bias leakage currents. The band diagrams do indeed match, and the one for this work is shown in Figure 47 below.

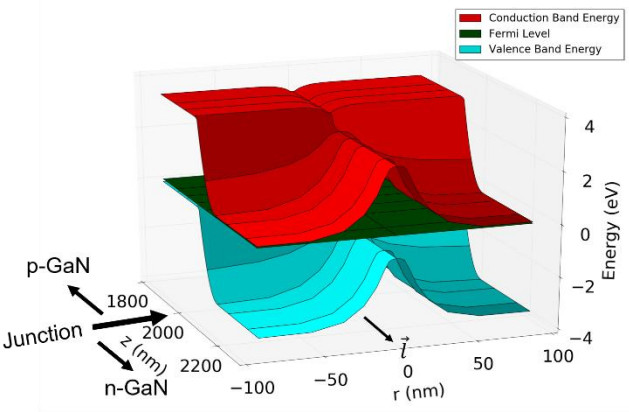


Figure 47: Equilibrium band diagram for the p-n junction in this work. This band structure matches our previously modeled p-n junctions observing forward bias leakage currents.

Upon confirmation of expected equilibrium band structure, the band diagram under 80 V reverse bias was analyzed and is shown in Figure 48. The dislocation maintains its band

distortion observed in equilibrium, but the band distortions due to the dislocation are small compared to the electric field across the junction.

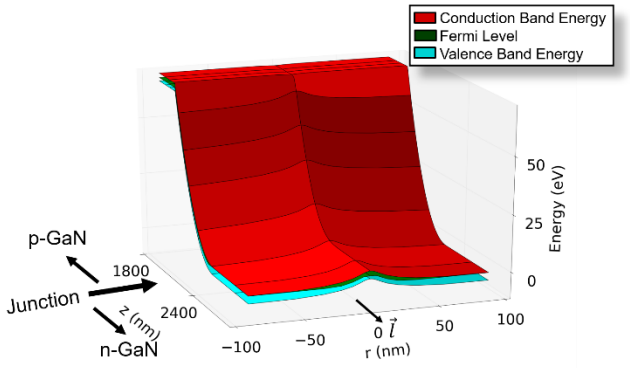


Figure 48: Band diagram for the modeled p-n junction under 80 V reverse bias. Note that the band distortions observed at equilibrium persist into reverse bias but are overshadowed by the bending of the junction due to the applied bias.

Since the mechanisms for leakage in reverse bias are inherently drift rather than diffusion related, the electric field profiles are considered and shown in Figure 49. In contrast to modeling forward bias characteristics, the electric fields are enhanced rather than diminished in reverse bias. This causes a peak in the electric field near the dislocation and junction due to the intersection of large components of the r- and z-components of the electric field. Recall that the recombination-generation due to TAT relates linearly to electric field, thus this peak in the electric field should generated electron-hole pairs that result in leakage.

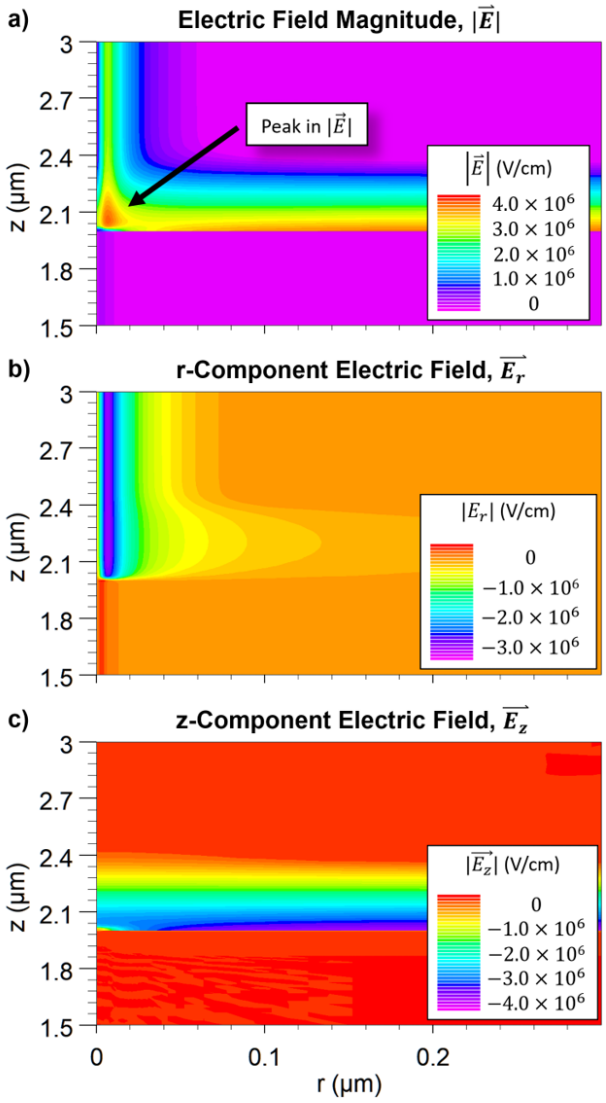


Figure 49: Electric field colormaps for the diode under study. a) The electric field magnitude - note the peak in electric field near the intersection of the dislocation with the junction. b) the radial component of the electric field. c) the z-component of the electric field.

In Figure 50, colormaps of the leakage currents are given as well as a recombination colormap on a linear scale. It shows that dislocation-mediated leakage current at reverse bias is driven by a generation of carriers at the peak electric field point. These e-h pairs are generated into a strong electric field that then sweeps the carriers apart with the holes going into the p-GaN and the electrons going into the n-GaN thereby resulting in a leakage current.

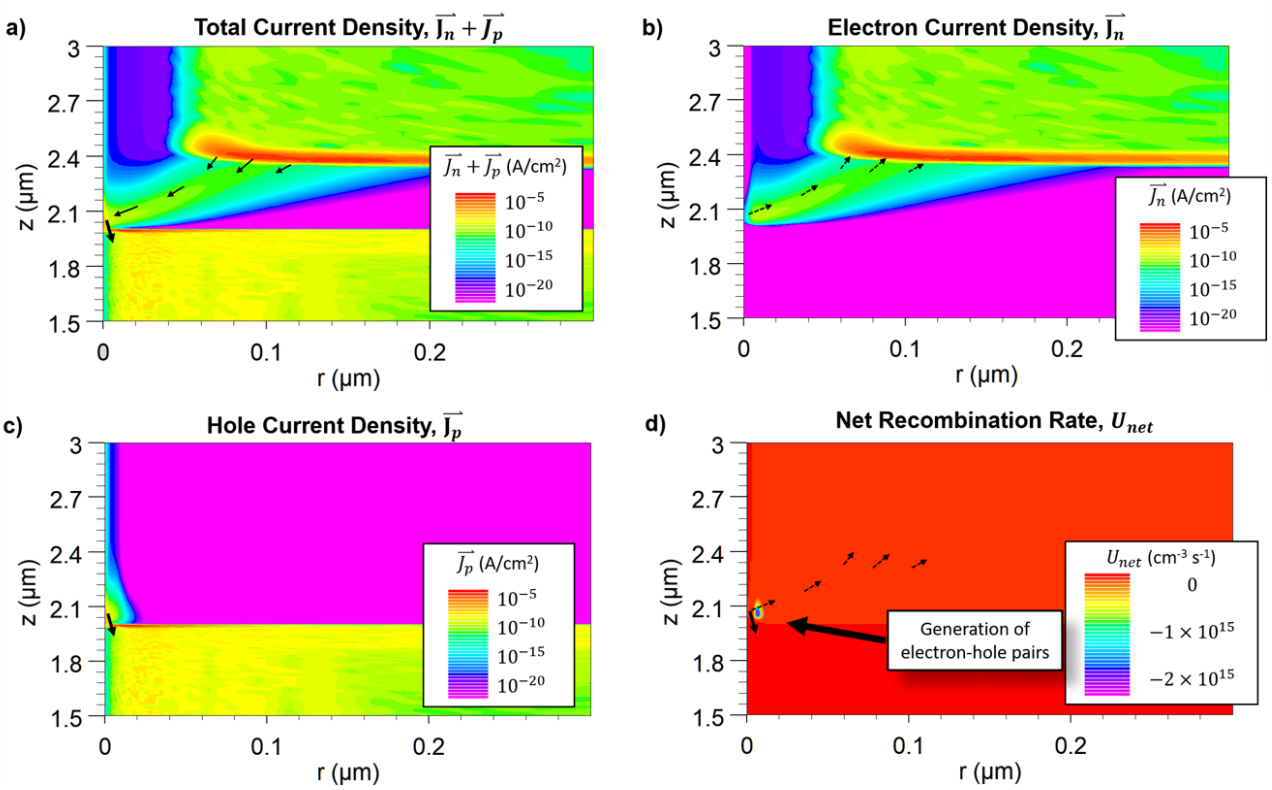


Figure 50: Leakage current color maps. a) The total conduction current density showing current flowing from the n- to the p-side of the junction. b) The electron current density showing that electrons are flowing from the dislocation-junction intersection towards the n-side bulk due to the high electric field. c) Hole current density showing a geometrically smaller region in which holes are flowing from the intersection into the nearby p-GaN region. d) The net recombination-generation colormap on a linear scale showing a sharp, negative region at the peak electric field. Negative values on this scale indicate that generation occurs in this region.

Finally, J-V curves comparing the reverse bias leakage currents of the diode studied in this work with different models were also plotted. In Figure 51, current densities are plotted with respect to the reverse bias voltage. The first comparative model removes the trap states completely from the model to simulate a diode with no dislocation in it – this is an ideal diode and should demonstrate no leakage current. The second comparative model keeps the dislocation-associated trap states in the model but removes the trap-assisted tunneling mechanism that appears to be essential to this leakage mechanism. In Figure 51, it can be

observed that both the diodes without the dislocation trap states and without TAT have leakage currents that are primarily characterized by noise. The dislocated sample with TAT included, however, displays a measurable leakage current after approximately 50 V reverse bias when the average reverse electric field is 1.7 MV/cm in the junction. Although this model hasn't been explicitly tested in the literature, the results are incredibly close to previous work conducted by Hurni et al.[40].

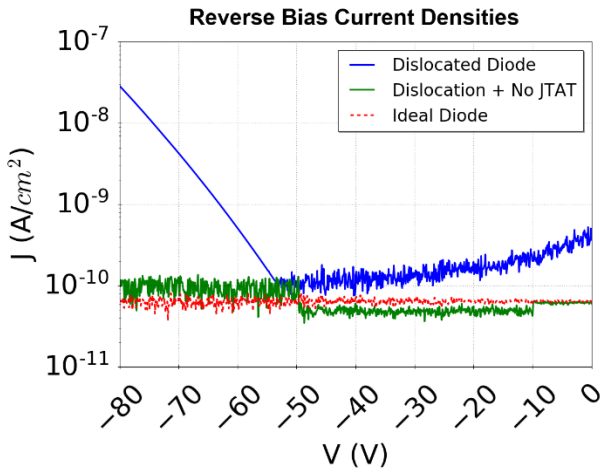


Figure 51: Reverse bias current density plots for the models under study. Note that the J-V curves for the model with no dislocation and with no trap-assisted tunneling are almost the same while the dislocated sample in this study demonstrates a measurable leakage current at applied biases greater than 50V. The onset of leakage currents in the dislocated diode corresponds with the appearance of measurable net generation due to the TAT mechanisms discussed in this work.

Summary

In this work, a vertical p-n diode with typical doping characteristics and an equivalent threading dislocation density of $10^8\ cm^{-2}$ was modeled in reverse bias. The model in this work uses a previously submitted model used to model forward bias leakage characteristics and adds an additional mathematical model to account for the effects of defects in high electric fields. The model shows that the dislocation-mediated leakage mechanism for reverse bias leakage in GaN p-n diodes is the generation of electron-hole pairs that are swept out of the

junction by the reverse bias electric field. This behavior results in a measurable leakage current within the model with behavior consistent with experimental values.

This article has been submitted for publication to Semiconductor Science & Technology.

Chapter 6. Summary & Future Work

In this dissertation, defect-mediated carrier transport mechanisms in vertical GaN p-n junctions has been studied experimentally and theoretically. Ca impurities were studied by growing comparative samples in an NH_3-MBE reactor and then processing them using a passivation process to prevent sidewall and p-GaN contamination. It was discovered that although Ca impurities do not have a substantial effect on the transport behaviors in a vertical GaN *p-n* diode relative to other factors such as threading dislocations, they do affect the bulk resistivity by acting as ionized impurity scattering centers or reducing hole concentration. Determining this more conclusively should be a priority for future work on this research and could be done by growing Hall samples with and without Ca to see how the Ca_i affects both mobility and hole concentration in a more rigorous, systematic way. Threading dislocation dependence was also experimentally verified and corroborated leakage behaviors observed in other growth methods such as PAMBE and MOCVD.

In conjunction with the threading dislocation experimental work, a model was designed and simulated to characterize the means by which threading dislocations cause leakage in vertical devices in both forward and reverse bias. It was discovered that in forward bias, the dislocation mediates a diffusion barrier reduction proportional to the doping of the diode that allows leakage current to bypass the barrier before the diode is "turned on." This bypass enabled an additional mechanism by which electrons and holes occupied the same region near the dislocation thereby increasing the np-product significantly; this catalyzed an additional leakage mechanism due to a region of high recombination rate near the dislocation. In reverse bias, the mechanism of leakage was discovered to be trap-assisted tunneling induced by the

high electric fields observed in reverse bias. This mechanism generates electron-hole pairs that are then swept out of the junction and thereby causing a leakage current to form.

Moving forward, there are many things that should be done both experimentally and theoretically to further this work. Experimentally, reducing processing- or growth-associated leakage needs to be top priority. To optimize this, the effect of growth interrupts, passivation materials, and contact metals needs to be understood. The growths in this work consistently had a 5 minute growth interrupt at the *p-n* interface where surface contaminants could ruin the integrity of the junction. Collaboration with other groups has indicated that SiN_x might be a better passivating material than SiO_2, but this material is also harder to etch – this will need to be explored in more detail. Lastly, switching from Al to Ti n-contact metal might make that contact more robust to process damage (particularly etching by the AZ NMP Rinse).

There are many spaces that can be explored within and around the simulations presented in this work. The biggest point of interest is the interaction between dislocations. To do this, a working 3D model of a dislocation needs to be made such that convergence can occur. Doing so could be done with the simple use of more raw computing power or better meshing and numerical methods can be formulated to make convergence more reliable. The main issue to be solved here is that in order to model a dislocation, a very fine resolution is required, but in order to see the full effects of a dislocation on the region around it, a very broad mesh is required. This requires either a very high number of mesh points such that solving the system becomes cumbersome or using a mesh resolution change to reduce the mesh points. Both of these solutions within the research discussed in this work resulted in models that failed to converge, thus 3D simulations of a single threading dislocation were not achieved. This must

be accomplished before such a model could incorporate two such structures to observe the interactions with one another.

The simulation results should be used to help design future experiments to confirm the validity of the model. An empirically and physically accurate model for the leakage of a *p-n* diode should be formulated based on the current model such that it considers interactions and externalities. Furthermore, the current model should be used to determine experiments that can verify its validity by altering parameters within the models that we can control such as threading dislocation density and doping. If certain parameters correlate to strong differences in model leakage, then these comparative device structures should be fabricated to assess the validity of the model presented.

This space could be further explored by using this model to construct simulations for threading dislocation effects within heterostructures such as LEDs. The effects of dislocations on things such as polarization and heterointerfaces could lead to interesting breakthroughs in understanding how these defects affect many device topologies used in the III-N alloy system. By understanding interactions between dislocations and heterostructures, this research would not only expand its scope substantially into a broader, more industrial scope, but it could also further deepen our understanding of how defects alter the electronic properties of III-Ns.

Appendices

Appendix A: Processing Optimization

Initial Process Optimization

The first sample processing path was designed following Dr. Hurni's prior work in this field[36]. This process involved the deposition of p-contacts as the initiation step to maintain p-contact Ohmic behavior by preventing any exposure of that surface to contaminants – mainly photoresist. By initiating process with the p-contact metal and then using a wet etch to create the appropriate contact areas, the sensitive interface between the p-GaN and contact metals would have minimal contamination. The entire process flow is given in **Figure 52**.

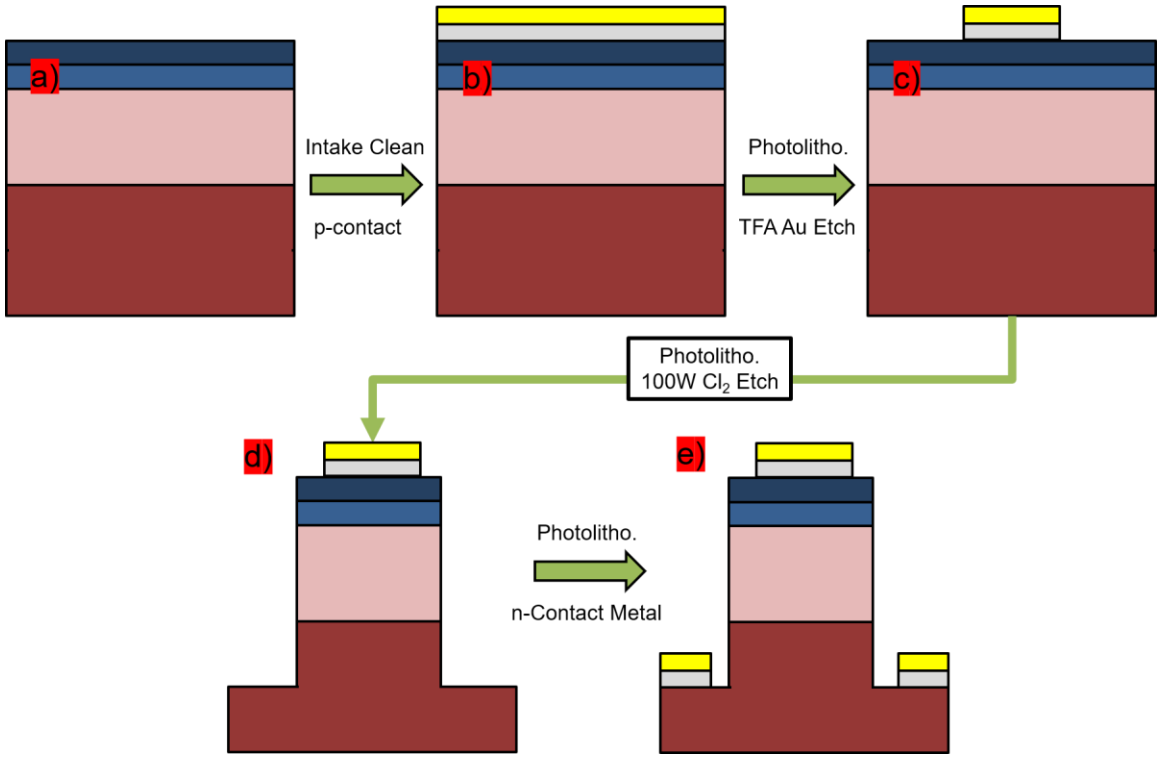


Figure 52: An overview of the process flow for the "Metal First" process used during the first year of this research. a) The bare epi of a p-n diode. b) Deposition of the blanket contact metal. c) A wet etch (Transene TFA Au Etchant) is used to define p-contact areas. d) Cl_2 dry etch in an RIE chamber to form isolation mesa structures. e) Deposition of patterned n-contact metal.

The first step of the process is an intake clean for the samples to remove any organic or loose contaminants. This is done by immersing the samples in a 150 mL of solvent contained 400 mL beakers using a 10 Sample Teflon™ wafer carrier made by the UCSB Physics Machine Shop. Each solvent has its own designated beaker for the purposes of minimizing cross-contamination between cleaning containers. Each step of the cleaning process consists of a 5' solvent bath in the room temperature (RT) high-power ultra-sonicator (HPUS) located in the solvent hoods of the cleanroom; the solvents used are acetone, methanol, and isopropanol, sequentially. The samples are then transferred to the acid bench in DI water using a designated DI water beaker. At the acid bench, the samples are immersed in HCl until the scheduled timeslot for metallization in E-Beam #3 (Temescal).

The samples are then loaded into the E-Beam #3 (Temescal) load / lock (LL) to begin contact metallization. The LL is pumped down to ~50 mTorr by a scroll pump and is then transferred into the main deposition chamber where the sample rests until the base pressure reaches $3 \times 10^{-6}\ torr$. Once base pressure is achieved, the p-contact metal stack (30 nm Pd / 300 nm Au) is deposited. The Pd is deposited at a deposition rate of 0.5 Å/s to initiate the contact interface and is then ramped up to 1 Å/s once 5 nm of metal has been deposited. The Au is then deposited immediately after the Pd concludes with a deposition rate of 2 Å/s that is then ramped up to 4 Å/s once 10 nm of Au has been deposited. After deposition of the Au contact layer is concluded, the sample is then removed from E-Beam #3 (Temescal) and transferred to the photolithography bay.

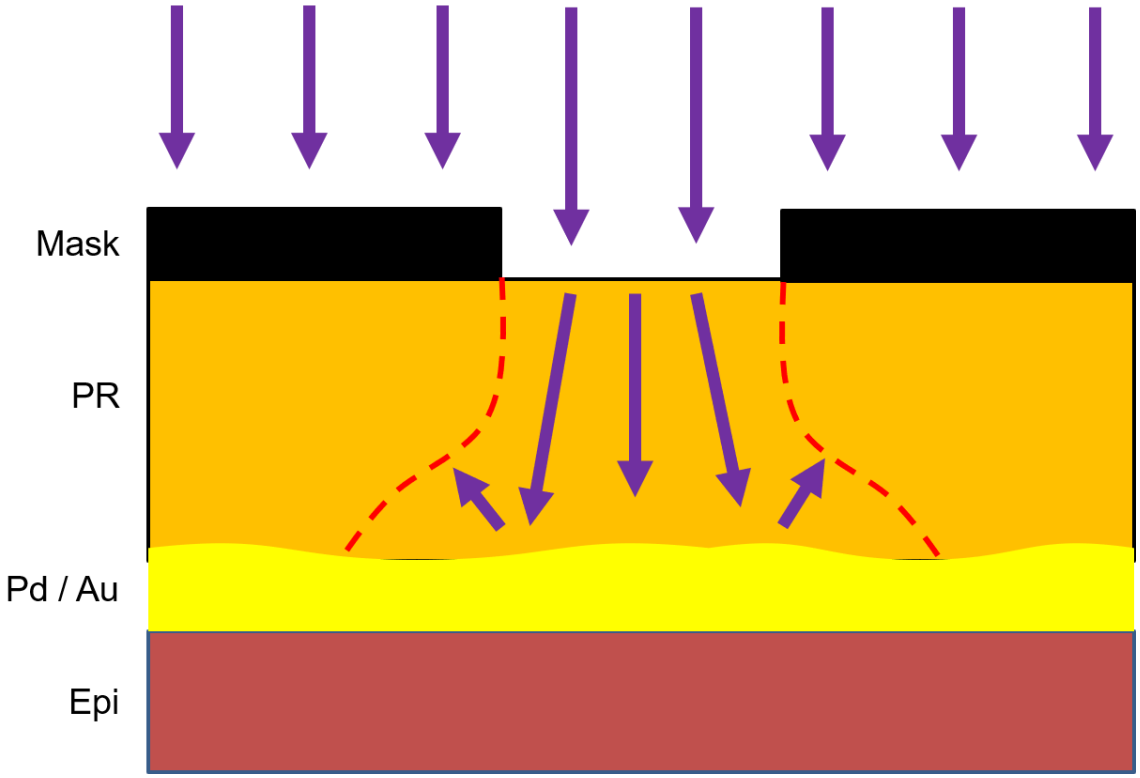


Figure 53: Schematic diagram showing the effect of reflective metal on the resolution of photolithography. Note that although the mask opening has a certain dimensionality, the area of material that is protected by the PR is slightly wider than the opening. In the case of openings < 10 μm, this can result in no opening in the PR being formed for metal etching.

In order to form geometric p-contacts, photolithography using nLoF-2020 photoresist (PR) and a wet etch of Transene TFA Au Etchant must be used. The standard recipe for nLoF-2020 was initially utilized, but this resulted in poor features for smaller contact rings and lines used in transmission line measurements (TLMs) despite such features remaining intact during calibration processing. This phenomenon was quickly attributed to the presence of Au on the photolithographic surface; since we were using a negative resist to open areas of Au for wet etchant to remove, the reflection of the UV used to form the lithographic pattern was reflecting off the metal and hardening thin regions of resist near the mask openings. This, in turn, resulted in regions where Au that should be exposed was protected by a thin layer of PR thus preventing removal of the metal (shown in **Figure 53**). By adjusting exposure times and adding a 30" O_2

plasma cleaning step, these issues were resolved. After p-contacts are formed, the PR is then removed by immersing the samples in AZ NMP Rinse at 80 °C for 4 hours. **It is incredibly important that the p-contact metal not be exposed to any high-power ultra-sonic – all cleaning processes done after the formation of p-contacts must not involve sonication of any kind. If p-contacts are exposed to sonication, they lose their Ohmic behavior due to the poor adhesion and sensitivity of the contact interface.** This behavior is due to a known issue regarding p-contact metals' (primarily palladium, platinum, and nickel) adhesion to the GaN surface. Exposing these weak interfaces due the energy of ultra-sonic treatment results in substantial damage that results in poor contact and device performance such as high contact resistance and burn-in behaviors.

Using the standard Nanofab photolithographic process for nLoF-2020, the samples were then patterned for the purposes of forming vertical mesas using reactive ion etching (RIE) with BCl_3 and Cl_2 plasmas inside of a PlasmaTherm RIE System. Before samples were etched, a chamber seasoning and an etch rate calibration was performed. The chamber seasoning was by performing a 30' O_2 plasma clean followed by a short, low-power BCl_3 plasma "chamber season"; this step is crucial in maintaining sidewall verticality and minimizing implant contamination into the sidewalls of the mesas. The etch rate calibration is performed by placing a thin piece of Si wafer over a piece of discarded GaN-on-Sapphire. This etch setup was loaded into the etch chamber and exposed to etching conditions for 10' and then removed to measure by a DekTak Profilometer. By normalizing the mesa height under the Si wafer to the etch time, an etch rate was found; this etch rate for a 100W Cl_2 etch was typically 73±3 nm/min. This result was highly consistent over the years and can be safely used as an approximation as of 2019. With an etch rate calibrated, the patterned sample is then loaded into the machine, and

an etch of appropriate depth is performed using the calibrated etch rate. The sample is then removed from the etch chamber and immediately immersed in DI water to remove Cl from the mesa sidewalls and improve device performance. The PR is then removed as before.

The final step in this flow is the deposition and metallization of the n-contacts. Patterning occurs as in the mesa etch photolithography, and the samples are immersed in a dilute mixture of HCl (DI:HCl 3:1) for 1’ to remove any metallic contaminants from the contact surface without damaging the lithographic patterning. The samples are then loaded into E-Beam #3 (Temescal) where they undergo the same pump down procedure noted for the p-contact metallization. The n-contact metal stack (30 nm Al / 300 nm Au) is then deposited using the same ramp rates discussed previously. The samples are then removed and immersed in AZ NMP Rinse at 80 °C for liftoff. As was previously noted, it is crucial that HPUS not be used once p-contacts have been formed; in most processes, HPUS provides much of the necessary force required to facilitate metal liftoff. In order to provide the force necessary for liftoff without resorting to HPUS, a large dropped is used to spray the sample surface with the AZ NMP Rinse. This action provides enough energy to remove the PR on the surface without damaging the underlying contact integrity. With the formation of the n-contacts, the diodes have been fabricated and are now ready for electrical characterization.

Initial Electrical Characterization

After fabrication, electrical data is measured on the DC Station in the High Frequency Measurements lab. Using needle probes, I-V curves for contact pads of different sizes are obtained. A 0V to 5V DC sweep with a 100mA compliance was the standard low-voltage measurement that was done to observe leakage and on-state characteristics.

Rectification was observed, but upon normalization with respect to area (a.k.a. the derivation of current density), it was discovered that the electrical current was not evenly distributed through the area of the devices as shown in Figure 54.

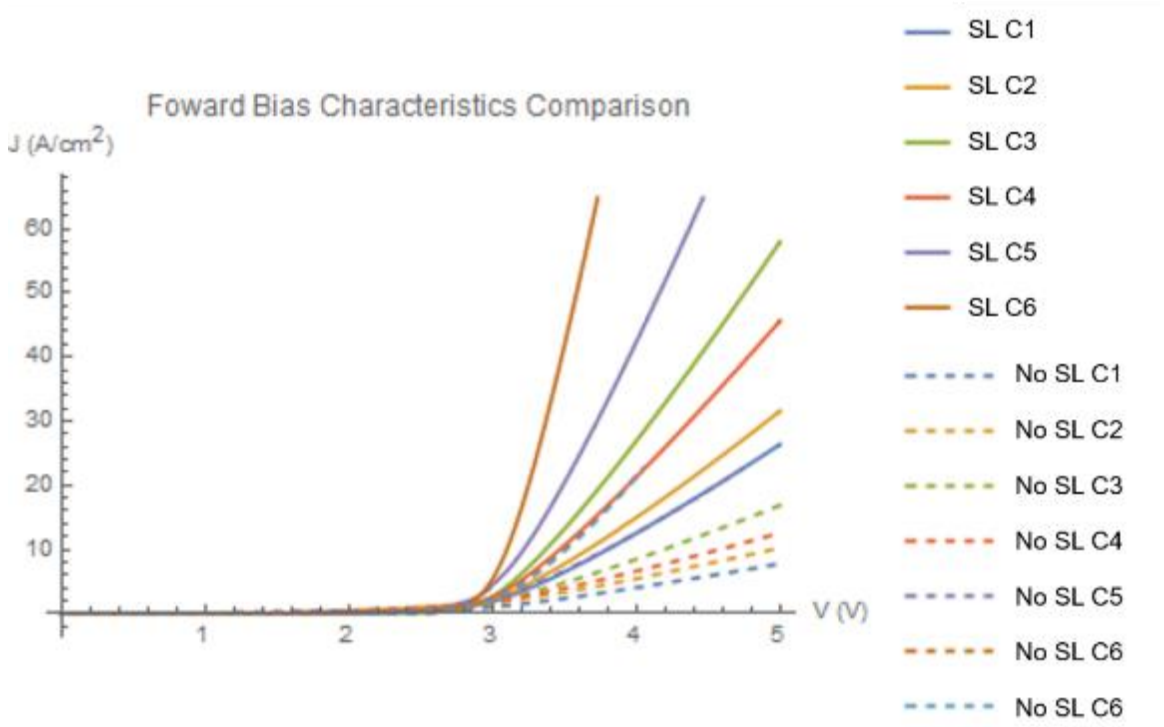


Figure 54: Current density vs. voltage plots of "Metal First" samples showing non-uniform current distribution through the device area. Note that the C# nomenclature indicates contacts of different sizes with small numbers the larger contact areas. Note that regions of smaller contact areas (a.k.a. higher perimeter-to-area ratios) have much higher current densities than the larger area contacts during turn-on.

Further analysis revealed that rather than current passing uniformly through the area of the device, it was confined to a 1D aspect of the device (Figure 55)– most likely the circumference. This behavior was consistent for the previously outlined “Metal First” process flow, thus it was concluded that this means of fabrication was resulting in a circumferential leakage path that needed to be addressed. Although no experimentation was done to confirm the source of the 1D leakage current, we hypothesized it was due to the migration of p-contact metal atoms to the sidewall due to the plasmonic environment of the RIE chamber. Cleaning procedures for

both the sample and the chamber were also revamped to be in line with other group procedures. To address this issue, a sidewall passivation scheme was formulated to ensure that current passed uniformly through the area of the diode rather than the perimeter.

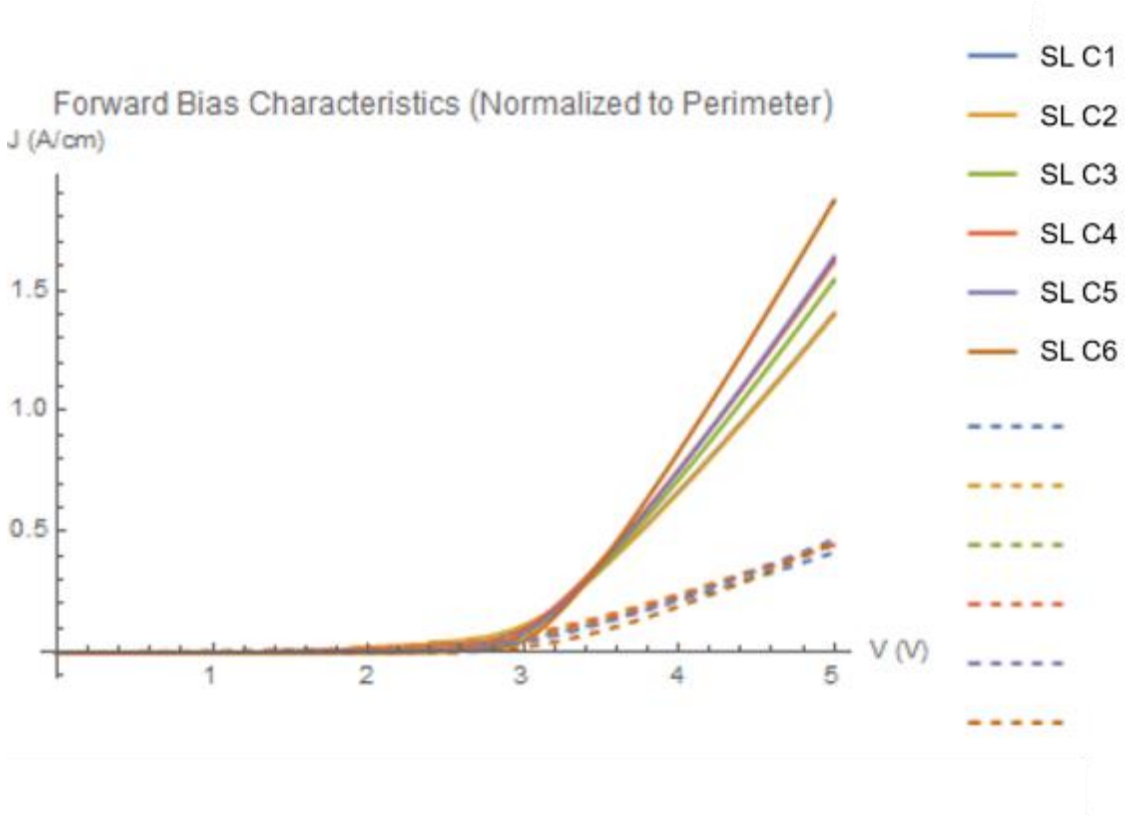


Figure 55: Linear current density vs. voltage showing that the current is evenly distributed over a 1D region of the device – most likely the perimeter.

Appendix B: Veeco 930 Operation Procedure Outline

1. Solvent clean samples in sonicator water bath
   a. 5’ Acetone with high-power ultrasonic (HPUS)
   b. 5’ Methanol with HPUS
   c. 5’ Isopropanol with HPUS – leave samples in Isopropanol until ready to load into blocks.
2. Load samples into blocks in the fume hood
3. Bake samples on Entry / Exit trolley in the Entry / Exit Chamber at 150 °C for 1.5 hours
4. Bake sample on Buffer Chamber Bake Station at 400 °C for 1 hour.
5. Load sample into the Main Chamber, rotate continuous azimuthal rotator (CAR) into the growth position, and set substrate heater to 450 °C

6. Once substrate heater is at 450 °C, put system into NH_3-Mode* and begin flowing 200 sccm NH_3 into the chamber.
7. Ramp substrate heater to growth temperature and proceed with desired growth.
8. During cooldown, maintain ≥ 50 sccm NH_3 flow to prevent GaN decomposition until substrate heater reaches 450 °C.
9. Remove sample from the chamber.

*** NH_3-Mode Check List**

- ✓ Cryopump gate valve closed.
- ✓ Ion pump gate valve closed.
- ✓ N_2 flowing through MC turbo
- ✓ MC ion gauge turned off
- ✓ Check MC load shutter and gate valve

Appendix C: Fabrication Flow (Detail)

Step Name	Substep Name	Tool	Param. #1	Param. #2	Param. #3	Param. #4
Pre-Passivation*	Solvent Clean	RT Sonicator (Max Setting)	5' Acetone	5' Methanol	5' Isopropanol	30" DI Water (Still)
	BHF Clean	HF Processing Bench	1' BHF Dip	1' DI Water (Running)		
	HCl Clean	Toxic / Corrosives Bench	1' Dip	1' DI Water (Running)		
Passivation	SiO2 Deposition	PECVD #1	SiO2 Coat	SiO2 Dep	50nm	1' 11"
PR #1	H2O Bake*	Hot Plate	115 C	3' Bake	1' Cool	
	PR Spin On	nLoF-2020	3000 RPM		30"	2.1 um
	Soft Bake	Hot Plate	110 C	90" Bake	1' Cool	
Litho #1	Exposure	MJB3 Aligner	i-Line Filter	14"	Mesa_Etch	
	PE Bake	Hot Plate	110 C	1' Bake	1' Cool	
	Develop	AZ300 Beaker	AZ300MIF	60" Dip	1' DI Water	**Very light stir**
O2 Plasma	O2 Descum	Plasma Asher	300 mTorr	100W	30"	
Oxide Etch	BHF Dip	HF Bench	~400nm/min	60" Dip	1' DI Rinse	**Very light stir**
Mesa Etch	Dry GaN Etch	RIE #5	O2 - BCl3 / Cl2 Season	Use the manufacturing		

				recipe (marked with a yellow star)		
		RIE #5	Speck / GaN High Power Etch		~73nm/min	
	DI Rinse	Wet bench	1' DI Water		Removes Cl from etch	
PR Removal*	AZ NMP Rinse	80 C Soniactor (Max Setting)	80 C Sonicator		Use dropper to agitate surface	
	Clean & Rinse	Wet bench	1' Isopropanol	1' DI Water		
Pre-Passivation	Solvent Clean	RT Sonicator (Max Setting)	5' Acetone	5' Methanol	5' Isopropanol	30" DI Water (Still)
Oxide Strip	BHF Dip	HF Bench	10'+ Dip	1' DI Water		
Passivation		PECVD #1	SiO2 Coat	SiO2 Dep	50nm	1' 11"
PR #2	H2O Bake	Hot Plate	115 C	3' Bake	1' Cool	
	PR Spin On	nLoF-2020	3000 RPM		30"	2.1 um
	Soft Bake	Hot Plate	110 C	90" Bake	1' Cool	
Litho #2	Exposure	MJB3 Aligner	i-Line Filter	14"	Mesa_Etch	
	PE Bake	Hot Plate	110 C	1' Bake	1' Cool	
	Develop	AZ300 Beaker	AZ300MIF	60" Dip	1' DI Water	**Very light stir**
O2 Plasma	O2 Descum	Plasma Asher	300 mTorr	100W	30"	
Oxide Etch	BHF Dip	HF Bench	~400nm/min	60" Dip	1' DI Rinse	**Very light stir**
p-Contact	Pd / Au Contact	E-Beam #3	30nm / 300nm	0.5 > 1 A/s	1 > 2 > 4 A/s	
PR Removal*						
PR #3	H2O Bake	Hot Plate	115 C	3' Bake	1' Cool	
	PR Spin On	nLoF-2020	3000 RPM		30"	
	Soft Bake	Hot Plate	110 C	90" Bake	1' Cool	
Litho #3	Exposure	MJB3 Aligner	i-Line Filter	14"	Mesa_Etch	
	PE Bake	Hot Plate	110 C	1' Bake	1' Cool	
	Develop	AZ300 Beaker	AZ300MIF	60" Dip	1' DI Water	
O2 Plasma	O2 Descum	Plasma Asher	300 mTorr	100W	30"	
Oxide Etch	Buffered HF Dip	HF Bench	~400nm/min	60" Dip	1' DI Rinse	
n-Contact	Al / Au Contact	E-Beam #3	30nm / 300nm		0.5 > 1 A/s	1 > 2 > 4 A/s
PR Removal*						

- Solvent Clean: Removes organic contaminants and loose particles.
- BHF Clean: Removes surface sub-oxides.
- HCl Clean: Removes metal contaminants.
- SiO_2 Passivation: 50 nm was found to be thick enough to protect the p-GaN surface but also thin enough to be consistently removed by a 1' BHF dip.
- If PR is started immediately after SiO2 deposition by PECVD, solvent cleaning is not necessary.
- PR Exposure: Longer than cited on Wiki. Optimization necessary as filter transmission properties change or other machine parameters on the MJB-3 contact aligners.
- **IMPORTANT**: Take samples out of AZ300MIF at 58" to account for the additional time needed to transfer to the DI rinse. Failure to do so results in overetch of fine (< 7 μm) features.
- RIE Season: This step is crucial to ensure mesa etch verticality and preventing implantation of contaminants into the sidewall.
- Pre-heat AZ NMP Rinse while metal contacts are being deposited to make liftoff more efficient.
- **IMPORTANT**: DO NOT SONICATE SAMPLE ONCE p-CONTACT IS ON THE SAMPLE. IT RESULTS IN POOR CONTACT QUALITY CONSISTENTLY

Appendix D: Backside Metallization & Temperature Control

It was discovered that over the course of a standard NH3-MBE growth, the backside metal being used (Ti) would undergo a chemical change into TiN_x. This was problematic for long growths as our pyrometry is calibrated for a surface temperature associated with a Ti backside metallization. By changing the backside Ti metal to TiN_x, the measurement is torpedoed in two ways – firstly, the emissivity of the metal at the probed interface changes, and secondly, the thermal transport and absorption properties of the backside metal are also changing. If temperature sensitive layers such as InGaN, AlGaN, or p-GaN were grown after a certain amount of time, their properties would deviate from the calibrated values since significant nitridation would not occur in the growth time for a simple calibration sample.

Before undertaking this work experimentally, three confirmation steps were undertaken to make sure that TiNx was indeed forming from the Ti. Firstly, literature was found confirming that TiNx has been grown in research using conditions similar to those found in our chamber

– namely, < 30 sccm of NH_3 and < 600 °C[58]. Secondly, the visual appearance of TiN_x was compared to TiN_x found on the market, and the golden-brown appearance shown in FIGURE did match with typical colorations for TiN_x thin films. Lastly, samples with this golden-brown material on the backside were submerged in HF, a strong Ti etchant. Even after 24 hours, the material had not been stripped providing irrefutable evidence that whatever was on the backside of these samples was not metallic Ti. This experiment was then followed by a dip in an HF/HNO_3 mixture, a known etchant of TiN_x, and the material rapidly etched from the sample.

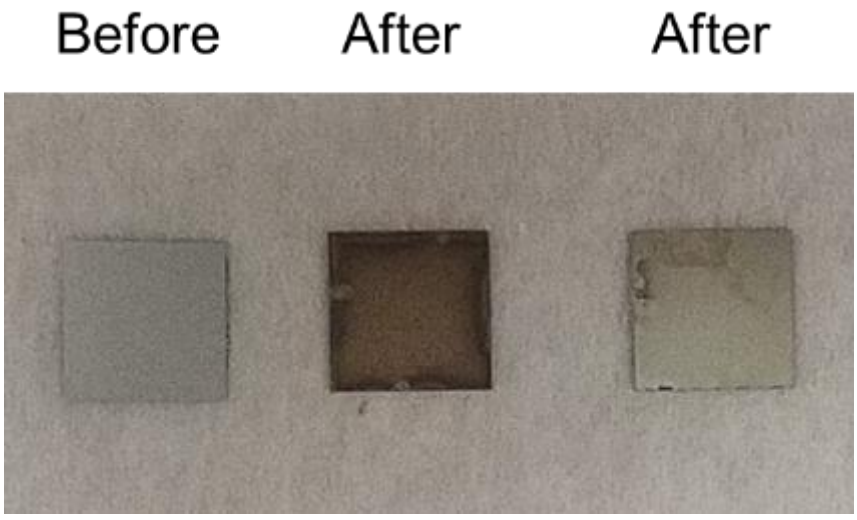


Figure 56: Sample comparisons showing the shift in backside appearance before and after growth as well as the uncontrollable variation in backside changes between different NH_3-MBE growths.

Figure 57: Image demonstrating characteristic delamination of backside Pd metal during process after growth.

With the confirmation of TiN_x coming reliably out of the NH3-MBE growth conditions, we elected to try Pd as a backside metallization in the chamber. Pd had three main advantages – high melting point, good thermal conductivity, and no readily formed nitride. The first issue encountered with this solution was the poor adhesion of Pd to the substrates. During dicing, approximately a third of samples were lost simply due to metal delamination due to the high-pressure water used during the process. Poor adhesion was also seen in the high heater temperatures necessary to reach growth conditions, for if the metal was not well attached to the substrate, the thermal transport to the surface will not be as efficient. Lastly, after growth, if the samples were processed chemically or mechanically, the metal always delaminated from the backside of the sample. In addition to adhesion issue, Pd would also lighten during the growth process; this lightening likely further exacerbated the high heater temperatures

necessary to achieve growth. In spite of all these issues with Pd backside metallization, the consistency of the metal-substrate interface did result in surprisingly good and consistent results in p-GaN quality and also demonstrated the knife edge on which the p-GaN growth condition rests as shown in **Table 10**.

Dopant Control	50%	50%	50%	50% + In
T_{sub} (ºC)	900	880	860	860
n / p (cm^{-3})	1.7e17	2.6e17	1.4e18	1.0e18
μ_n (cm^2 / V-s)	4.1	10.0	5.3	10.4
R_{sh} (Ω/ □)	289,900	66,000	28,000	19,400
ρ (Ω - cm)	9.0	2.5	0.81	0.58

Table 10: p-GaN calibrations with the NH_3 stable Pd backside metallization. Note the rapid loss of hole concentration within a 20 °C shift. This indicates that the p-GaN growth condition is highly sensitive to temperature and is certainly affected by prior uncertainty in the pyrometry precision due to TiN_x formation.

We also, without optimization, managed to grow consistently record quality p-GaN with high hole concentrations and mobilities further indicating the necessity for more reliable temperature control in the growth of p-GaN material in NH3-MBE.

In order to now solve the poor adhesion problem, a very thin Ti interlayer was added to assist in adhesion to the surface. This layer required optimization between metal adhesion and infrared interference. If the metal was too thin, it would not interfere with the optical measurement of pyrometry if it underwent any chemical changes, but it also would not adequately adhere the Pd to the substrate. Conversely, if the Ti was too thick, the Pd would adhere very well to the substrate, but it would then be optically relevant and make the

measurement vulnerable to chemical changes due to the growth environment. Thus, an experiment was conducted by which four samples of Al_2O_3 were coated with 500 nm Ti, 500 nm Pd, 1 nm Ti / 500 nm Pd, and 5 nm Ti / 500 nm Pd. These samples were diced and then loaded into the reactor. In the main chamber, each sample was loaded separately and heated up to approximate growth temperature by using a typical growth power (300W) and allowed to settle its temperature for 1 hour with no NH_3 flowing. The NH3 was then, at t = 0 sec, flowed into the system at a high rate (500 sccm), and the pyrometer temperature was measured at regular intervals to monitor the thermal stability of the metal stack. The results are shown in **Figure 58**.

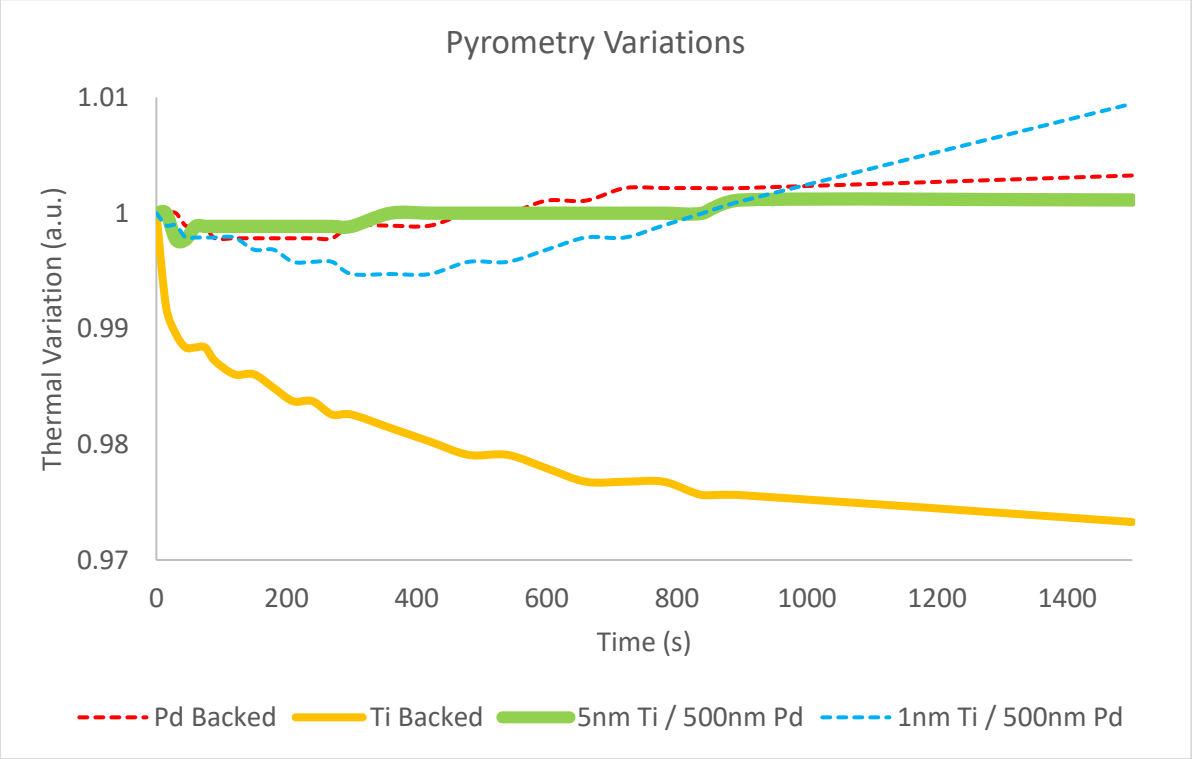


Figure 58: Measured variations in pyrometer readings for Al2O3 samples with different backside metallization. The 5 nm Ti / 500 nm Pd showed the greatest temperature stability relative to the other samples.

From this experiment, we concluded that a 5 nm Ti interlayer was optimal for achieving growth temperature stability.

The last phase of this problem was to solve the high powers required to achieve growth temperatures. In order to achieve this, we then added a 100 nm Ti layer on top of the Pd layer in order to maximize optical absorption of the CAR infrared. By structuring the backside metal in this stack, the measurement interface is protected and stable while the top layer of Ti ensures strong thermal coupling with the substrate heater. This is now the metal stack that is used in all growths on our reactor.

Appendix E: Dislocation Modeling Details

Before discussing the details of the model that was used to simulate a dislocation in a p-n junction, it seems important to first discuss the constraints on the problem and how this limited our options for solutions. The main issue is that a threading dislocation is a 3D structure with a 6-fold rotational symmetry about the dislocation core (approximately). Thus, ideally, a model addressing this issue would also be in 3D; however, the issue that arises here is that of resolution and convergence. The dislocation itself is a very small feature that requires a very fine mesh resolution to accurately model; the electronic effects of the dislocation, however, are very large on the order of 100 nm, and the junction itself will require even greater radial distance to accurately model (~500nm). To model this 3D requires a theoretically simple mesh that was attempted, but these models did not converge due to the immense and relatively rapid variation in the mesh resolution to model the problem such that there was a manageable number of points for the resources available to us. Thus, in order to model a threading dislocation, a 2D model was necessary, but it had to consider cylindrical symmetry in order to accurately model the 3D behavior of the crystal around the defect. Furthermore, we have access to a select number of software simulation suites at UCSB and were hopeful that one of them would be adequate to model this problem. Eventually, we discovered that Silvaco's ATLAS simulation

suite could use cylindrical coordination to model a 2D slice of a symmetric system, and this was the ultimate reason that our models are done in this environment.

Within the Silvaco DeckBuild code environment, the model for this research was conducted. The first step in constructing the model was to define a mesh of nodes that would be used in the Finite Element Analysis. In **Table 11** and **Table 12** the resolution parameters for the model's radial and z-component meshes are given, respectively.

Location	$r_0\ (\mu m)$	$r_f\ (\mu m)$	$\Delta r\ (\mu m)$
Dislocation Core	*0*	*0.005*	*0.001*
Perfect Crystal	*0.005*	*0.564*	*0.05*

Table 11: Radial mesh parameters used in modeling a dislocation. Note that a radius of 0.564μm was used to approximate a TDD of 10^8 cm^{-2}. Also note that the Δr given is the final resolution of the of the region. The software automatically smoothens the transition between regions to avoid creating mesh discontinuities.

Location	$r_0\ (\mu m)$	$r_f\ (\mu m)$	$\Delta r\ (\mu m)$
n-GaN	*0*	*0.49*	*0.1*
Junction	*0.49*	*0.51*	*0.005*
p-GaN	*0.51*	*1.0*	*0.1*

Table 12: Z-component mesh parameters used in modeling a dislocation.

The mesh definition given in the above tables results in the mesh given in Figure 59. With the mesh in place, the regions and properties are then set as described in 0. Chapter 4. Defect Characterization.

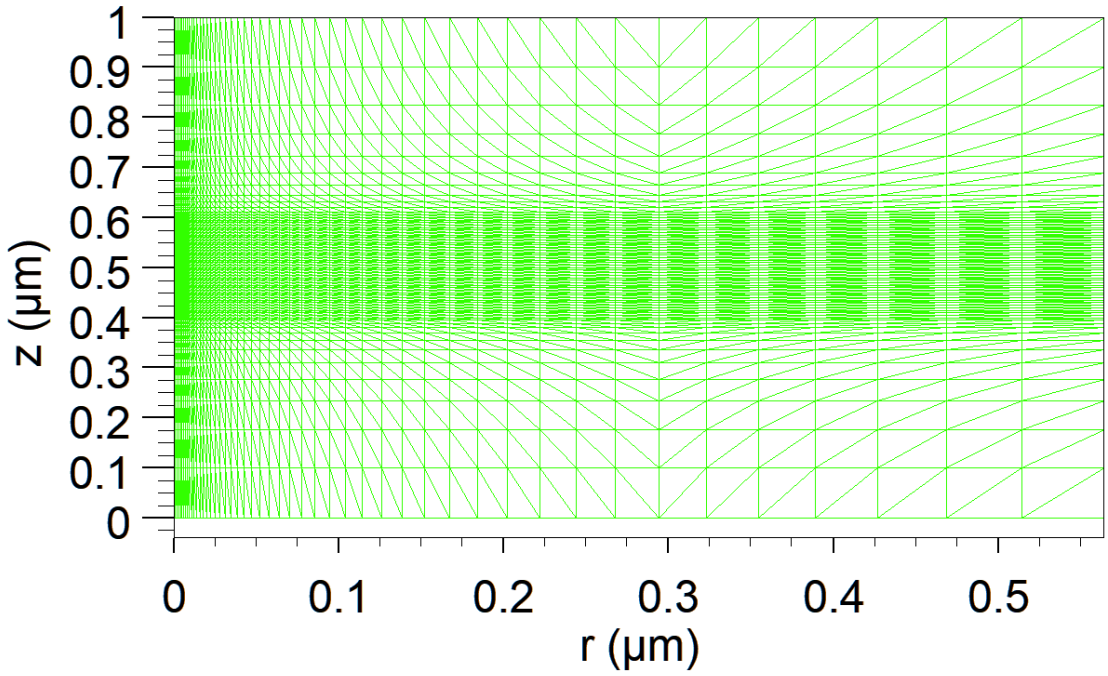


Figure 59: Mesh structure for dislocation modeling demonstrating variability in mesh resolution required for accurate modeling and convergence.

Finally, below the code that was used to model these diodes is given to allow for future projects on this topic to have a solid base from which to work.

```
GO       ATLAS

MESH     SPACE.MULT=1.0                  CYLINDRICAL
SET      TDD=CONTROL_XSEC_NTMAX
SET      MESH_LIM=0.564
SET      P_TRAP_LEV=2.3
SET      N_TRAP_LEV=2.5
SET      FWHM=0.003
SET      TRAP_DENS=6.84E19
SET      NA=5E19
SET      ND=5E17
SET      CAP_X_SEC=1E-12
SET      TNP=1E-12

# FWHM IS NOT PRECISELY THE 'CHARACTERISTIC' TAG

# RADIAL MESH - [0NM, 5NM] [5NM, 600NM]
```

```
# IT'S BUMPING THE MESH FOR SOME REASON. HELPFUL BUT UNKNOWN AS TO HOW OR WHY.
X.MESH      LOCATION=0.0          SPACING=0.001
X.MESH      LOCATION=0.005        SPACING=0.001
X.MESH      LOCATION=$MESH_LIM    SPACING=0.05

# 564NM RADIUS ~ 10^8CM-2 TDD

# Z MESH - [0, 2000NM]
Y.MESH      LOCATION=0.0 SPACING=0.1
Y.MESH      LOCATION=0.5 SPACING=0.005
Y.MESH      LOCATION=0.5 SPACING=0.005
Y.MESH      LOCATION=1.0 SPACING=0.1

# REGIONS 1 & 3 - N- & P-TYPE TD REGION
# REGIONS 2 & 4 - N- & P-TYPE BULK REGION

REGIONNUMBER=2    MATERIAL=GAN      X.MIN=0.0    X.MAX=$MESH_LIM    Y.MIN=0.0
      Y.MAX=0.5
REGIONNUMBER=4    MATERIAL=GAN      X.MIN=0.0    X.MAX=$MESH_LIM    Y.MIN=0.5
      Y.MAX=1.0

# CONTACT ELECTRODES - AL FOR N-CONTACT & PD FOR P-CONTACT
ELECTRODE   NUMBER=1    NAME=ANODE TOP    MATERIAL=ALUMINUM
ELECTRODE   NUMBER=2    NAME=CATHODE      BOTTOM    MATERIAL=PALLADIUM

# DOPING
DOPINGREGION=2    UNIFORM    N.TYPE CONC=$ND
DOPINGREGION=4    UNIFORM    P.TYPE CONC=$NA

# CHANGE DOPING FROM TAUN / TAUP BASED TO SIGN / SIGP BASED WITH CROSS SECTION = 2E-
12 CM-2
#DOPING      TRAP  ACCEPTOR    E.LEVEL=$N_TRAP_LEV
      CONCENTRATION=$TRAP_DENS      GAUSSIAN      CHARACTERISTIC=$FWHM      \
#           DEGEN=1               TAUN=$TNP  TAUP=$TNP  DIRECTION=X  Y.MIN=0.0
      Y.MAX=0.495  X.MIN=0.0
#
#DOPING      TRAP  DONOR       E.LEVEL=$P_TRAP_LEV
      CONCENTRATION=$TRAP_DENS      GAUSSIAN      CHARACTERISTIC=$FWHM      \
#           DEGEN=1       TAUP=$TNP  TAUN=1E-9  DIRECTION=X
      Y.MIN=0.505  Y.MAX=1.0    X.MIN=0.0

DOPINGTRAP  ACCEPTOR    E.LEVEL=2.7  CONCENTRATION=$TRAP_DENS      GAUSSIAN
      CHARACTERISTIC=$FWHM      \
            DEGEN=1               SIGN=$CAP_X_SEC    SIGP=$CAP_X_SEC
      DIRECTION=X  Y.MIN=0.0    Y.MAX=0.5    X.MIN=0.0
```

```
DOPINGTRAP DONOR E.LEVEL=$P_TRAP_LEV CONCENTRATION=$TRAP_DENS
        GAUSSIAN CHARACTERISTIC=$FWHM \
                DEGEN=1 SIGN=$CAP_X_SEC SIGP=$CAP_X_SEC DIRECTION=X
        Y.MIN=0.5 Y.MAX=1.0 X.MIN=0.0

# INCOMPLETE IONIZATION PARAMETERS
MATERIAL MATERIAL=GAN EAB=0.19 EDB=0.025 GCB=2
        GVB=4 TAUN0=1E-9 \
                        TAUP0=1E-9 NSRHN=1E17 NSRHP=1E19

# ADJUST MOBILITY AND LIFETIMES IN REGIONS TO GET ~200NM MINORITY DIFFUSION LENGTHS
MATERIAL MUN=32 MUP=8 TAUN0=4.8E-10 REGION=4
MATERIAL MUP=26 MUN=400 TAUP0=5.6E-10 REGION=2

#
#
#
#
# STRUCTURE SET UP FINISHED
#
#
#
#

## WITH TRAPS
MODELS PRINT INCOMPLETE SRH FERMIDIRAC TEMPERATURE=300 AUGER
#TRAP.JTAT JTAT.M2=1E-23

# SOLVE USING BLOCK THEN THE NEWTON METHODOLOGIES FOR ENERGY BALANCE
CALCULATIONS
METHOD GUMMEL NEWTON CARRIERS=2
# PX.TOL=1E-7 CX.TOL=1E-7

# OUTPUT PARAMETERS
OUTPUT CON.BAND VAL.BAND E.FIELD ELEC.EFF.FLD ELEC.EFF.VEL
        E.LINESE.MOBILITY ERRORS IMPACT\
        J.DRIFT J.DIFFUSION J.TOTAL RECOMB TRAPS
        U.AUGER \
        U.BBT U.RADIATIVE U.SRH U.TRAP QFN QFP
        CHARGE TRAPS.FT

PROBE CON.BAND
PROBE J.CONDUCTION
PROBE J.ELECTRON
PROBE J.HOLE
PROBE J.TOTAL
```

```
PROBE  AUGER
PROBE  CHARGE
PROBE  CONDUCTIVITY
PROBE  FIELD  DIR=-90
PROBE  GENERATION
PROBE  N.CONC
PROBE  P.CONC
PROBE  R.TRAP
PROBE  RADIATIVE
PROBE  RECOMBIN
PROBE  SRH

SOLVE  INITIAL
SAVE   OUTF=ZERO_BIAS_$"TDD".STR

LOG    OUTFILE=FORWARD_BIAS_$"TDD".LOG      CSVFILE=FWD_BIAS_$"TDD".CSV
#SOLVE       VCATHODE=0.0      VSTEP=0.05    VFINAL=1.2    NAME=CATHODE
#SAVE  OUTF=12V_FWD_$"TDD".STR
SOLVE  VCATHODE=0.0      VSTEP=0.1     VFINAL=2.4    NAME=CATHODE
SAVE   OUTF=24V_FWD_$"TDD".STR
SOLVE  VCATHODE=2.4      VSTEP=0.1     VFINAL=3.2    NAME=CATHODE
#SOLVE       VCATHODE=2.9      VSTEP=0.1     VFINAL=3.2    NAME=CATHODE
SAVE   OUTF=32V_FWD_$"TDD".STR
LOG    OFF
```

Appendix F: Table of Values for Dislocation Modeling

Sym.	Description	Value	Units
k	Boltzmann constant	8.62×10^{-5}	eV / K
σ_n	Capture cross section – electrons	1×10^{-12} [44]	cm^2
σ_p	Capture cross section – holes	1×10^{-12} [44]	cm^2
$\bar{n}$	Capture rate – electrons	N/A	s^{-1}
$\bar{p}$	Capture rate – holes	N/A	s^{-1}
N_A	Concentration – acceptor dopants	5×10^{19}	cm^{-3}
N_D	Concentration – donor dopants	5×10^{17}	cm^{-3}
n	Concentration – electrons	N/A	cm^{-3}
Q_T	Concentration – charged trap states	N/A	
p	Concentration – holes	N/A	cm^{-3}
n_i	Concentration – intrinsic carriers	3.43×10^{-10}	cm^{-3}
N_A^-	Concentration – ionized acceptor dopants	N/A	cm^{-3}
N_{tA}^-	Concentration – ionized acceptor traps	N/A	cm^{-3}
N_D^+	Concentration – ionized donor dopants	N/A	cm^{-3}
N_{tD}^+	Concentration – ionized donor traps	N/A	cm^{-3}
ρ_T	Concentration – trap states*	N/A	cm^{-3}

J_n	Current density – electrons	N/A	A/cm^2
J_p	Current density - holes	N/A	A/cm^2
ϵ_r	Dielectric constant	8.9	---
N_C	Effective density of states – conduction band	2.2×10^{18}	cm^{-3}
N_V	Effective density of states – valence band	4.2×10^{19}	cm^{-3}
m_n^*	Effective mass – electron	1.98×10^{-31} ($0.2m_0$ [59])	Kg
m_p^*	Effective mass – holes	1.28×10^{-30} ($1.4m_0$ [60])	Kg
ψ	Electric potential	N/A	V
q	Electron charge	1.61×10^{-19}	C
e_n	Emission rate – electrons	N/A	s^{-1}
e_p	Emission rate – holes	N/A	s^{-1}
E_A	Energy level – acceptor	0.19 [50]	eV
$\underline{E_C}$	Energy level – conduction band edge	N/A	eV
E_D	Energy level – donor	0.025 [50]	eV
E_{Fn}	Energy level – electron quasi-Fermi	N/A	eV
E_{Fp}	Energy level – hole quasi-Fermi	N/A	eV
E_i	Energy level - intrinsic	1.73	eV
E_V	Energy level – valence band edge	N/A	eV
c	Lattice parameter – c-component	5.186	Å
τ_n	Lifetime – electrons	N/A	s
τ_p	Lifetime – holes	N/A	s
M^2	Matrix element for JTAT	10^{-23}	V^2/cm^3
μ_n^{maj}	Mobility – majority electrons	400	$\frac{cm^2}{Vs}$
μ_n^{min}	Mobility – minority electrons	32	$\frac{cm^2}{Vs}$
μ_p^{maj}	Mobility – majority holes	8	$\frac{cm^2}{Vs}$
μ_p^{min}	Mobility – minority holes	26	$\frac{cm^2}{Vs}$
ϵ_0	Permittivity of free space	8.85×10^{-14}	F/cm
U	Recombination rate - net	N/A	s^{-1}
U_{SRH}	Recombination rate – Shockley-Read-Hall	N/A	s^{-1}
R_{SC}	Screening radius	N/A	nm
g_n	State degeneracy – conduction band	2	---
g_p	State degeneracy – valence band	4	---
T	Temperature	300	K
v_n	Thermal velocity – electrons	2.60×10^7	cm / s
v_p	Thermal velocity – holes	9.87×10^6	cm / s
$f(E_T)$	Trap state occupancy	N/A	---

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